StarFive 赛昉科技

StarFive JH7110 Datasheet

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Legal Statements

Important legal notice before reading this documentation.

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Preface

About this guide and technical support information.

About this document

This document mainly provides the users with the basic introductions and features for StarFive next generation SoC platform - JH7110.

Revision History

Table 0-1 Revision History

Version	Released	Revision
1.61	2023/8/2	Corrected minor errors in datasheet, including GMAC pin voltage and UART note location.
1.60	2023/7/14	Updated the boot device to QSPI + SD/eMMC.
1.59	2023/6/19	Updated datasheet per JH7110 tuning result including specs and notes change in eMMC, I2C, S7, and so on.
1.55	2023/6/7	Added known issue of recommended DDR rate to 2,133 Mbps instead of 2,800 Mbps - Set DDR/LPDDR to 2,133 *(on page 102)*. Added the maximum size of DDR and LPDDR of 8 GB - DDR *(on page 16)*. Added notes to eMMC and SD interfaces that the max speed is DDR50 (50 MHz) - eMMC Interface *(on page 17)* and SD/MMC Interface *(on page 18)*.
1.54	2023/5/31	Updated CAN-FD to CAN in Clock Structure *(on page 83)* to avoid misleading. CAN-FD is only partially supported, thus removed from the datasheet.
1.53	2023/5/12	Updated Video decoder frame rate to 4K@30fps.
1.52	2023/4/25	Removed the incorrect DDR max capacity. See AVL list for a complete and most updated list of whether your device or peripheral is supported.
1.51	2023/3/29	Minor updates in certain signal descriptions.
1.5	2023/2/2	Added Pin Delay information for hardware product design reference.
1.4	2023/1/16	Added the power consumption specification in standby mode based on real test. Removed descriptions of 2 x 2D1C descriptions in MIPI channel DPHY support to avoid possible misleading information.
1.3	2022/12/6	Added the chapter of Known Issue and describes the issue of GMAC limitation within the chapter.
1.2	2022/10/20	Modified after the internal review. Refined block diagram. Updated spec details on MIPI and PCIe.
1.1	2022/09/15	Modified after the internal review. Updated spec details. Added SDIO note per FAE comment.
1.0	2022/09/05	First official release of the document.

Notes and notices

The following notes and notices might appear in this guide:

- **Tip:**
  Suggests how to apply the information in a topic or step.

- **Note:**
  Explains a special case or expands on an important point.

- **Important:**
  Points out critical information concerning a topic or step.

- **CAUTION:**
  Indicates that an action or step can cause loss of data, security problems, or performance issues.

- **Warning:**
  Indicates that an action or step can result in physical harm or cause damage to hardware.

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1. System Overview

1.1. Introduction

JH7110 is a high-performance RISC-V SoC featuring high-performance, low-power-consumption, rich interface options, and powerful image and video processing capabilities.

JH7110 is equipped with a 64-bit high-performance quad-core RISC-V processor core sharing 2 MB of cache coherency, whose working frequency is 1.5 GHz. JH7110 has a rich high-speed native interface, supports the Linux operating system, and has powerful image and video processing system. The StarFive ISP is compatible with mainstream camera sensors, built-in image/video processing subsystem supports H.264/H.265/JPEG codec. The integrated GPU makes its image processing capabilities stronger, such as 3D rendering. With high-performance, OpenCL/OpenGL ES/Vulkan support, JH7110 can further enhance intelligence and efficiency. JH7110 can complete a variety of complex image/video processing and intelligent visual calculations. Also, it meets multiple visual real-time processing requirements at the edge.

1.2. Block Diagram

The following figure shows the block diagram of JH7110.

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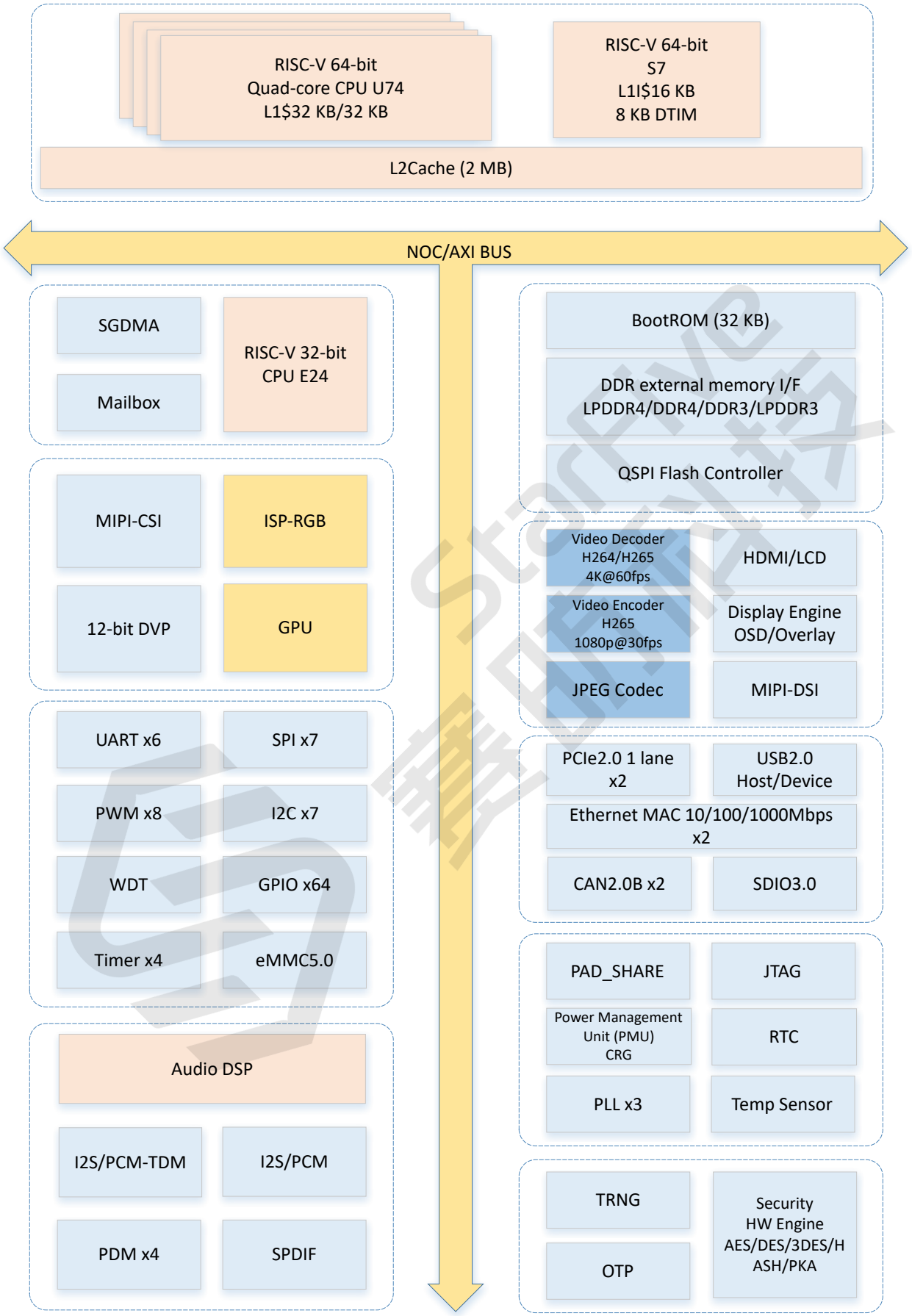
Figure 1-1 Block Diagram



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Note:

- JH7110 supports one USB port. One of the PCIe2.0 lanes can be shared by USB3.0.
- JH7110 supports one port for SDIO and one port for eMMC, or both ports for SDIO.

1.3. Application

An introduction to the application scenarios.

JH7110 applies to the following scenarios.

- Commercial Electronics
  - Personal *Single Board Computer (SBC)*
  - Home NAS
  - Router (Soft routing)
  - Notebook computer
- Smart Home
  - Sweeping robot
  - Intelligent home appliances
  - Video surveillance
- Industrial Intelligence
  - Industrial robot
  - Unmanned store

1.4. Highlighted Feature

JH7110 has the following highlighted features.

- RISC-V U74 quad-core and S7 monitor core with 2 MB L2 cache
- Support Linux OS with kernel versions 5.10 and 5.15
- CPU work frequency up to 1.5 GHz
- GPU IMG BXE-4-32
- 32-bit LPDDR4/DDR4/LPDDR3/DDR3, up to 2,800 Mbps
- Video decoder supports up to 4K@30fps and multi-stream for H.264/H.265
- Video encoder supports up to 1080p@30fps and multi-stream for H.265
- Provide JPEG encoder/decoder
- Support up to 1080p@30fps full-functional ISP
- Support video input: 1 × DVP and 1 × MIPI-CSI with 4D1C up to 4K@30fps
- Support video output: MIPI display output with 4D1C up to 1080p@60fps
- Support 1 × HDMI2.0 port display up to 4K@30fps
- Support 24-bit RGB parallel interface up to 1080p@30fps
- Support 2 × PCIe2.0, 1 lane
- Support USB3.0 Host/Device (By reusing 1 of the PCIe2.0 lanes)

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- Support 2 × Ethernet MAC 1,000 Mbps, 2 × CAN2.0B
- Support IEEE 1588-2002 and IEEE 1588-2008 standards
- Support TRNG and support OTP, DMA, QSPI, and other peripherals
- Dedicated audio processing and sub-system

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2. Feature

2.1. CPU Subsystem

The CPU subsystem of JH7110 has the following features.

2.1.1. Overview

The CPU subsystem of JH7110 has the following features.

- 64-bit High-performance RISC-V CPU (U74) quad-core for main general computing
- 32-bit RISC-V CPU (E24) core for low power and control/configure tasks as a coprocessor

2.1.2. U74 MC

The U74 quad-core of JH7110 has the following features.

- Fully compliant with the RISC-V ISA specification
- 4 × RV64GC U74 Application Cores
    - 32 KB L1 I-cache with ECC
    - 32 KB L1 D-cache with ECC
    - 8 Region Physical Memory Protection
    - Sv39 Virtual Memory support with 38-bit (Physical Address)
- 1x RV64IMAC S7 Core
    - 16 KB L1 I-Cache with ECC
    - 8 KB DTIM with ECC
    - 8 Region Physical Memory Protection
- U74 and S7 cores are fully-coherent
- Integrated 2 MB L2 Cache with ECC
    - The L1 Instruction Cache and the L2 Cache can be configured into high-speed deterministic SRAMs
- Real-time Capabilities, and internal time counting integrated
- Debug with instruction trace

Note:
S7 is only used for BOOTROM.

2.1.3. E24 Core

The E24 core of the JH7110 has the following features.

- Fully compliant with the RISC-V 32 ISA specification
- RV32IMFC E24 Core
    - 16 KB I-cache with 32 Byte cache line
    - 4 Region Physical Memory Protection

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- CLIC with support for up to 127 interrupts with 16 priority levels
- Support JTAG as Debug port
- Support AHB-Lite system bus for 2 GB memory map

2.1.4. SGDMA

The SGDMA (DMA) of JH7110 has the following features.

- Support general DMA operations and Scatter Gather DMA
- Support up to 4 gather&scatter channels
- Support up to 32 requests
- Support AXI4 bus width of 64-bit
- Support memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral transfer
- Can generate both interrupts for transmission completion and for transmission failure due to errors
- Support arbitration - fixed and round robin
- Provide status information of each transfer for each channel in the status register

2.2. Memory and Storage

2.2.1. On-Chip Memory

The On-Chip Memory of JH7110 has the following features.

- BootROM up to 32 KB

2.2.2. DDR

The DDR of JH7110 has the following features.

- DDR controller
  - DDR4/3 and LPDDR4/3 modes and signaling, rates up to the speed of 2,800 Mbps
  - The maximum size of DDR4/3 and LPDDR4/3 is 8 GB
  - Internal deskew PLLs for high speed, low jitter clock generation (clk4x)
  - x16/x32 data path interface extendable
  - DRAM ranks of 1, 2 (could be asymmetric)
  - Bank-interleaving and rank-interleaving (symmetric ranks only)
  - Support for dynamic DRAM frequency scaling
  - Automated clock gating of internal logics
  - Error-correction code (SECDED) to select DRAM memory space
  - Address region-based security control support
  - Automated low power control of DRAM devices
  - AMBA AXI4 protocol for main data path interface for DDR controller
  - AMBA APB4 protocol for configuration register access interface for DDR controller
  - Flexible refresh control

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        - Automated adjustment of the refresh interval
        - Pulled-in or postponed refreshes
        - Dynamic per-bank / all-bank refresh switching
        - Opportunistic advanced per-bank refresh
    - Open page based advanced page policy
        - Programmable timeout pre-charge
        - Auto pre-charge for reducing command congestion
    - Independent read and write timing adjustments with auto-calibration
    - Various power-down modes for low power including self-refresh support
    - DFI 4.0 specification between DDR controller and DDR PHY
- DDR PHY
    - High resolution write/read timing control
    - Per-bit deskew on the write data path
    - Per-bit deskew on the read data path
    - Support for multiple leveling/training modes through PHY evaluation mode
    - Register programming interface to all PHY parameters
    - PHY independent mode training logic
    - Write/read data timing per-chip select
    - Low-power modes
    - Low-speed test interface (PHY BIST)
    - At-speed ATPG support (OPCG)
    - DBI support
    - PHY controller frequency ratio of 2:1
    - IO calibration
    - JTAG interface
    - Boundary-scan support
    - Testability features

2.2.3. QSPI

The QSPI of JH7110 has the following features.

- Programmable master mode
- Data rate up to 100 Mbps
- 1/2/4 data-bit and 2-chip-select
- Support XIP mode and boot mode
- Separate data input and output bit

2.2.4. eMMC Interface

The eMMC Interface of JH7110 has the following features.

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- Support eMMC 5.0/SD 3.0
- Support 4-bit and 8-bit eMMC data width
- Support 512B block size
- Support devices with capacity up to 256 GB
- Support speed mode: Legacy/High SDR/High DDR/HS200
- Identification mode
- MMC full-speed mode
- MMC high-speed mode
- MMC DDR mode

Note:
Due to the lack of high speed IO, the eMMC supports up to the speed of HS200 (50 MHz clock rate).

2.2.5. SD/MMC Interface

The SD/MMC interface of JH7110 has the following features.

- Compatible with SD3.0
- Support SD/SDHC/SDXC, with SDXC capacity 32 GB - 2 TB.
- Compatible with MMC5.0
- Support 4-bit data width
- Support the following speed modes:
  - DEFAULT
  - HIGHSPD
  - UHSI_SDR12

Note:
Due to the lack of high speed IO, the SD/MMC supports up to the speed of SDR12 (25 MHz clock rate).

2.3. Image Subsystem

2.3.1. Camera MIPI IN/OUT Interface

The camera MIPI IN/OUT interface of JH7110 has the following features.

- CSI-2 RX Controller
  - Support of the MIPI CSI-2 v1.3 protocol over DPHY PPI interface up to a maximum of 4 ×1.5 Gbps
  - Support Pixel interface
  - Byte to pixel conversion one-pixel interface
  - Direct memory dump using packed byte operation
  - Flow control
  - Payload FIFO operation
  - Monitoring of frame for automatic start/end of frame synchronization when enabled

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- Extended Functions for Virtual Channel extension and RAW16/20 modes as defined for MIPI CSI-2 V2.0 Specification
- Can be enabled by setting the V2P0_SUPPORT_ENABLE bit in the STATIC_CFG configuration register
- Support the data types of RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, and RAW20
- Virtual Channel Extension (VCX) is employed - Effects ECC handing

- MIPI RX DPHY
  - Support standard 8b PPI interface compliant of MIPI DPHY Spec.
  - Support 1 clock lane and up to 4 Data Lanes scalability in DPHY mode.
  - Support HS-Rx data rate from 80 Mbps up to 1.5 Gbps. (DPHY)
  - Support LS-Rx data rate of 10 Mbps and ultra-low-power mode.
  - Support Triggers, ULPS, and LPDT.
  - Support on-die terminated and non-terminated operation with switchable termination integrated.
  - Support fault detection of sequence error. (Error report)
  - Support clock and data lane swapping function.
  - Build-in BISTTX for at-speed testing

2.3.2. ISP-RGB

The ISP-RGB of JH7110 has the following features.

- Sensor Interface
  - Support up to 1080P @30fps CMOS RGGB image sensor with the output format of RAW
  - Support 1 MIPI and 1 DVP sensor input interface
  - Support 12-bit sensor data input
- Image processing engine
  - Built-in color pattern generation
  - Sensor black level compensation
  - Defective pixel correction
  - R/G/B LUT for sensor linearisation correction
  - Image analysis for AE, AWB, and AF
  - Programmable histogram analysis
  - White balance control
  - Lens shading compensation
  - Color shading compensation
  - CMOS sensor spatial crosstalk cancellation (Gr and Gb balance filter)
  - Advanced Bayer CFA color interpolation
  - False-color suppression
  - Advanced edge control and enhancement
  - R/G/B Gamma LUT
  - Color correction matrix
  - Color space conversion

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    - Brightness/contrast and hue/saturation adjustment
    - Global tone mapping
    - Spatial noise reduction
- Back-end processing
    - Seamless digital scale down from 1/4 × to 1 ×
    - Support up to 3 channel video streaming

Note:
5M Px is only supported with the following data path "Sensor → VIN (max 4K) → DDR", the sensor data output is YUV420 or YUV 422.

2.3.3. GPU

The GPU of JH7110 has the following features.

- IMG BXE-4-32 MC1 with work frequency up to 600 MHz (400 MHz by default)
- Fully compliant with the following APIs:
    - Support OpenCL 3.0
    - Support OpenGL ES 3.2
    - Support Vulkan 1.2
- Tile-based deferred rendering architecture for 3D graphics workloads, with concurrent processing of multiple tiles
- Programmable high-quality image anti-aliasing
- Fine-grain triangle culling
- Support for DRM security
- Support for GPU visualization
    - Up to 8 virtual GPUs
    - Support for IMG Hyper-Lane technology, with 8 hyper-lanes available
    - Separate IRQs per OSID
- Multi-threaded Unified Shading Cluster (USC) engine incorporating pixel shader, vertex shader, and GP-GPU (compute shader) functionality
- USC incorporates an ALU architecture with high SIMD efficiency
- Fully virtual memory addressing (up to 64 GB address space), supporting unified memory architecture
- Fine-grained task switching, workload balancing, and power management
- Advanced DMA driven operation for minimum host CPU interaction
- System Level Cache (SLC)
- Specialized Texture Cache Unit (TCU)
- Compressed texture decoding
- Lossless and/or visually lossless low area image compression - the Imagination
- frame buffer compression and decompression (TFBC) algorithm
- Dedicated processor for B-Series core firmware execution
    - Single-threaded firmware processor with a 2 KB instruction cache and a 2 KB data cache.

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2.4. Video Subsystem

2.4.1. Video Encoder

The video encoder of JH7110 has the following features.

- H.265 Encoder, 1080p@30fps
- I/P slices
- CTU64
    - Supported Prediction Unit (PU) size: 16 × 16, 8 × 8
    - Supported Transform Unit (TU) size: 16 × 16 to 8 × 8
- Parallel tools
    - Multi-slice: Independent slice segment and a dependent slice segment
- High-performance CABAC encoding
- In-loop de-blocking filtering
- Loop filtering across the slice
- Lossless coding
- Noise reduction
- Rate Control
    - VBR, CBR, and ABR
    - ROI support

2.4.2. Video Decoder

The video decoder of JH7110 has the following features.

- 1-channel 4K@30fps or 8-channel 1080p@30fps
- Support Format 420, 8-bit/10-bit
- Support I/P type slice
- H.265 Main/Main10, L5.1 up to 4096 × 2160@60fps
- H.264 High/High10, L5.2 up to 4096 × 2160@60fps
- 128bit AXI Bus interface
- Support Lossless Compression for frame buffer to save bandwidth
- Frame-based Processing promises the lowest burden to the host processor for video operation
- Generating an interrupt when(ever) a specified number of MB-/CTU-rows are reached for low delay decoding
- H.264 decoding tools including:
    - Compatible with the ITU-T Recommendation H.264 specification
    - Support MVC Stereo High Profile
    - Support CABAC
    - Support CAVLC
    - Variable block size (16 × 16, 16 × 8, 8 × 16, 8 × 8, 4 × 8, and 4 × 4)

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- Interlaced coding tools are NOT supported
- FMO/ASO is NOT supported

- H.265 decoding tools include:
  - Compatible with ISO/IEC 23008-2 high-efficiency video coding
  - I/P slices
    - All intra-prediction modes
    - All inter-prediction modes
  - Variable CTU size: 64 × 64 to 16 × 16
    - Variable Transform Unit (TU) size: 32 × 32 to 4 × 4
    - Variable Prediction Unit (PU) size: 64 × 64 to 4 × 4
  - Advanced Motion Vector Prediction (AMVP) and merge mode
  - ¼ Motion compensation with 8 tap filters
  - Uniform reconstruction quantization (URQ)
  - High-performance CABAC decoding
  - In-loop de-blocking filtering
  - Sample Adaptive Offset (SAO)
  - Loop filtering across slice/tile boundaries
  - Data reporting to the external host
  - Robust error concealment
  - Sequence change detection

2.4.3. JPEG Codec

The JPEG Codec of JH7110 has the following features.

- 290 MPixel/sec for YUV420, 210 MPixel/sec for YUV422, 140 MPixel/sec for YUV444
- Bit rate 480Mbps (MJPG 8M 30fps 422 1:8)
- Baseline/Extended sequential ISO/IEC 10918-1 JPEG compliance
- Compliant with Motion JPEG
- Support 1 or 3 color components
- 8-bit or 12-bit samples for each component - configurable
- Support 4:2:0, 4:2:2, 4:4:0, 4:4:4 and 4:0:0 color format (Maximum 6 8 × 8 blocks in 1 MCU)
- Support from 16 × 16 pixels to 32K × 32K (32,768 × 32,768)
- Support ROI (Region of Interest) - decoder only
- Support 422/444 packed mode for all color formats
- After conversion to 422/444 color format
- Value-added Features for Encoding
  - Partial mode for encoding
  - On-the-fly rotator/mirror
- Value-added features for decoding

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- Partial mode for decoding
- ROI (Region of Interest)
- On-the-fly rotator/mirror
- On-the-fly downsample

2.5. Display Subsystem

The display subsystem, named as DOM_VOUT_TOP in system, includes display controller and display interfaces, such as RGB IF, HDMI and MIPI.

2.5.1. Display Controller

The display controller of JH7110 provides the following features.

- DP: RGB101010, RGB656, RGB666, RGB888 output formats
- DPI: RGB101010, DPI_D16/18/24 output formats
- Pixel inputs accepted from multiple RGB and YUV formats
- Color Space Conversion BT.2020 and BT.709
- Pixel output is up to 30-bit RGB in multiple formats
- Support ARGB888 and Mask cursor formats
- A separate Look-Up Table for Dither
- A separate Look-Up Table for Gamma Correction
- Overlay with coordinate generator with 6 image layers shared by 2 display panels (screens)
- Alpha Blending: 8 Porter Duff Blending modes
- Vertical and horizontal scaling
- Horizontal 3/5 tap; vertical 3 tap
- Programmable filter order
- 15.16 fixed point scaling factor
- Default display: 1080p
- Maximum display: 4K2K
- Independent sync and blank signals for each display
- Independent gamma and dither tables for each display
- Support 24-bit RGB parallel display interface up to 1280 × 720p@60fps or 1920 × 1080p@30fps

2.5.2. HDMI2.0 Interface

The HDMI interface of JH7110 has the following features.

- Compliant with HDMI2.0, HDMI1.4, and DVI1.0 specifications
- Up to 6 Gbps per data channel
- Support YUV4:4:4, YUV4:2:2, YUV4:2:0 and RGB4:4:4 video format
- Support 8/10/12-bit color depth
- Support standard I2C master interface for DDC interface

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- Support programmable output swing, termination, and pre-emphasis
- Support 8-channel I2S for audio, and up to 192 KHz audio sampling rate
- Support display resolution up to 4K@30fps

2.5.3. MIPI Display Interface

The MIPI display interface of JH7110 has the following features.

- MIPI TX DPHY
  - Support standard 8-bit PPI interface compliant with MIPI specifications.
  - Support 1 Clock Lane and up to 4 Data Lanes scalability.
  - Support HS-Tx data rate from 80 Mbps up to 2.5 Gbps. (Per lane)
  - Support LP-Tx data rate of 10 Mbps.
  - Support LP-Tx ULPS and LPDT.
  - Support reverse direction ULPS and LPDT.
  - Support on-die transmitter termination.
  - Support clock and data lane swapping function.
  - Minimalized lane-to-lane skew of multi-data lanes.
  - Smaller frequency step supports more power efficiency of the whole DPHY ecosystem.
  - Built-in LDO with 1.2 V voltage output to meet LS-Tx DC spec.

2.6. Connectivity Subsystem

2.6.1. PCIe2.0

The PCIe module of JH7110 has the following features.

- PCIe2.0 Controller
  - Support 2 PCIe2 .0 x1 interface with 2 PCIe2.0 controller
  - Support link rate of 2.5, 5.0 GT/s per lane, and 32-bit PIPE interface
  - PHY Interface for PCI Express (PIPE), Revision 4.4.1/5.1.1 compliant
  - Designed for Endpoint, Rootport, and dual-mode/shared silicon
  - 128-byte maximum payload size
  - 1 Virtual Channel (VC)
  - Up to 64 Physical Functions (in Endpoint mode)
  - Configurable Receive and Transmit buffer size
  - Advanced Error Reporting (AER) support
  - ECRC generation and check support
  - Integrated Clock Domain Crossing (CDC) to support user-selected frequency for the Bridge
  - Lane reversal support
  - Alternate Routing ID Interpretation (ARI)
  - Legacy PCI Power Management support

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    - Clock and power gating support
    - Native Active State Power Management L0s and L1 state support
    - Power Management Event (PME message)
    - MSI (up to 32) and INT message support
    - MSI-X Capability support
    - Latency Tolerance Reporting (LTR)
    - L1 PM Substates with CLKREQ
    - SR-IOV support with up to 512 virtual functions
    - Address Translation Service, including Page Request interface
    - Process Address Space ID (PASID)
    - VPD Capability support
    - TLP Processing Hints
- PCIe2.0 PHY
    - Compatible with PCIe/USB3/SATA base Specification
    - Fully compatible with the PIPE3.1 interface specification
    - Data rate configurable to 1.5G/2.5G/3G/5G/6G for different application
    - Support 16-bit or 32-bit parallel interface when encode/decode enabled
    - Support 20-bit parallel interface when encode/decode bypassed
    - Support flexible reference clock frequency
    - Support 100 MHz differential reference clock input or output (optional with SSC) in PCIe Mode
    - Support Spread-Spectrum clock (SSC) generation and receiving from -5000ppm to 0ppm
    - Support programmable transmit amplitude and De-emphasis
    - Support TX detect RX function in PCIe and USB3.0 Mode
    - Support Beacon signal generation and detection in PCIe Mode
    - Support Low-Frequency Periodic Signaling (LFPS) generation and detection in USB3.0 Mode
    - Support COMWAKE, COMINIT, and COMRESET (OOB) generation and detection in SATA Mode
    - Support L1 sub-state power management
    - Support RX low latency mode in SATA operation mode
    - Support Loopback BERT and Multiple Pattern BIST Mode

2.6.2. USB

The USB module of JH7110 provides the following features.

- 1 × USB2.0/3.0 controller (port)
    - USB Interface:
        - Compliant with USB 3.0 Specification
        - Compliant with xHCI 1.0 Specification
        - SuperSpeed, Hi-Speed, and Full-Speed supported
        - Single USB2.0 Port

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        - Single USB3.0 Port (By reusing 1 of the PCIe2.0 lanes)
        - USB 3.0 PIPE interface compliant
        - USB 2.0 UTMI+ interface compliant
        - USB2 L1/L2 Support
        - USB3 U1/U2/U3 Support
    - Application Interface:
        - AXI4 Master Interface with 64-bit data and 32-bit address
        - APB4 Slave interface with 32-bit data and address
    - Dual Mode Operation:
        - HW selectable default mode selection supporting operation without any SW interaction
        - Programmable runtime mode change
        - Host Negotiate Protocol (HNP) support
        - SRP support
        - Provide separate power domains for host and peripheral device logics
    - Host Mode (CDNSXHCI):
        - Support configurable total slots (maximum of 32)
        - 32 endpoints per slot
        - Support 256 Primary Streams
        - MSI Support
        - Root Hub functionality implemented
        - xHCI Dynamic and Static Low Power Management Support
        - xHCI DMA engine with 64-bit @ 125 MHz Full Duplex Data Path
    - Peripheral Mode (USBSS-DEV):
        - Support 8 endpoints for both read and write, and Endpoint #0 supports control transfers
        - Scatter-gather DMA
        - Dynamic data buffering
    - Integrated Protocol Stack
        - Memory integration
        - Clock, reset and power management integration
- USB2.0 PHY
    - Compliant with USB2.0 and USB1.1 specification
    - Compliant with UTMI Specification Version 1.0
    - Support HS (480 Mbps)/FS (12 Mbps)/LS (1.5 Mbps) modes
    - All required terminations, including 1.5 K Ω pull-up on DP and DM, and 15 K Ω pull-down on DP and DM are internal to the chip
    - 16-bit, 30 MHz or 8-bit, 60 MHz parallel interface for HS/FS
    - Serializing for transmitting data stream and De-serializing for receiving the data stream
    - USB Data Recovery and Clock Recovery on receiving
    - Integrated Bit Stuffing and NRZI encoding for Transmit

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- Integrated Bit Un-Stuffing and NRZI decoding for Receive
- SYNC and EOP generation on transmit packets and detection on receive packets
- Support termination calibration with the external resistor
- Support scan test of digital block
- Built-in self-test for production testing
- Support USB suspend state and remote wakeup
- Support detection of USB reset, suspend and resume signaling
- Support high-speed identification and detection as defined by USB 2.0 Specification
- Support high-speed host disconnection detection

2.6.3. Ethernet GMAC

The Ethernet GMAC module of JH7110 has the following features.

- Compliant with IEEE 802.3 specifications
- Support for IEEE 1588-2002 and IEEE 1588-2008 standards including:
  - IEEE 802.3-az for Energy Efficient Ethernet (EEE)
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion.
  - IEEE 802.1Q VLAN tag detection for reception frames
- Support data transfer rates of 10/100/1,000 Mbps auto-negotiation using the following PHY models
  - YT8521DH/DC
  - YT8531DH/DC
- Support data transfer rates of 1,000 Mbps only using all other PHY models
- Multiple TCP/IP offload functions supported

Power Management Module (PMT) with remote wake-up frame and magic packet frame processing options

- RGMII interface to communicate with an external gigabit PHY.

2.6.4. SDIO Interface

The SDIO Interface of JH7110 provides the following features.

- Support up to 2 SDIO 3.0 interfaces
- Compatible with SDIO3.0 protocol
- Support 4-bit data width

2.6.5. CAN2.0B

JH7110 supports the following CAN2.0B features.

- Support 2 CAN2.0B interfaces
- Support CAN2.0B specification
- Data rates up to 5 Mbps
- Programmable baud rate pre-scaler (1 to 1/256)
- Separate clock domains for host interface and CAN protocol machine

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- Configurable receive buffer and Two Transmit Buffers
- Independent and programmable internal 29-bit acceptance filters
- Time-stamping:
  - ISO 11898-4 Time-Triggered CAN with partial hardware support
  - CiA 603 time-stamping

2.7. Audio Interface

2.7.1. PCM TDM

The PCM TDM of JH7110 has the following features.

- Support short frame sync, long frame sync and multi-slot mode
- Multi slot supported, and up to 16 slots
- Slot width including 8-bit, 16-bit, 20-bit, and 32-bit
- Sample rate up to 192 KHz, and data transferred with system DMA
- Support master and slave mode, and software configurable

2.7.2. I2S

The I2S of JH7110 has the following features.

- 2 × I2S transmitters, and 1 for HDMI audio
- 1 × I2S receiver to receive data from internal PDM or from external audio I2S ADC
- Support programmable sample rate: 16 K/44.1 K/48 K/96 K/192 KHz
- Data resolution support 16-bit (programmable)
- Programmable FIFO depth up 64 for each channel
- Support to select between master and slave modes, software configurable

2.7.3. SPDIF

The SPDIF of JH7110 has the following features.

- Provide 2 sets of SPDIF, 1 for RX and 1 for TX mode
- Support sample rates from 16 KHz up to 192 KHz.
- Support PCM format with a resolution of 16-bit per sample

2.7.4. PDM

The PDM controller of JH7110 has the following features.

- Support up to 4 PDM channels (MICs) with the same sample rate
- Pulse Density Modulation interface for digital MIC interface
- 128 oversample ratio, output sample clock: 62.5 KHz to 6.144MHz (48KHz)
- Combine clock source for each 2 channels
- I2S interface connect with I2S RX internally in slave mode

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2.8. Security Subsystem

2.8.1. Encrypt Engines

The encryption engines of JH7110 has the following features.

- AES
  - Support encryption and decryption
  - Support 128-bit/192-bit/256-bit of key size
  - Support ECB/CBC/CFB/OFB/CTR/CCM/GCM operation modes
  - Support SCA countermeasure
  - Support DMA mode
- DES/3DES
  - Support standard DES with 64(56)-bit of key size
  - Support 3-DES with 128(112)-bit or 192(168)-bit of key size
  - Support ECB/CBC/CFB/OFB operation modes
  - Support SCA countermeasure
  - Support DMA mode
- HASH
  - Support SHA0/1
  - Support SH224/256/384/512
  - Support HMAC_SHA0/HMC_SHA1
  - Support HMAC_SHA224/256/384/512
  - Support DMA mode
- PKA
  - Support modular addition from 32-bit to 2048-bit with granularity of 32-bit
  - Support modular subtraction from 32-bit to 2048-bit with granularity of 32-bit
  - Support modular multiplication from 32-bit to 2048-bit with granularity of 32-bit
  - Support modular exponentiation from 32-bit to 2048-bit with granularity of 32-bit
  - Support Montgomery modular multiplication from 32-bit to 2048-bit bits with granularity of 32-bit
  - Support up to 512-bit of point addition/double under prime field
  - Support SCA countermeasure
- ECC for 512-bit

2.8.2. TRNG

The TRNG module of JH7110 provides the following features.

- Ring-oscillator based entropy source
- Support LFSR based digital post process
- Support self re-seeding
- 256-bit random number generation

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2.8.3. OTP

The OTP module of JH7110 provides the following features.

- VDD and VDD2 power supply: 0.9 V VDD, 1.8 V VDD2 for reading and programming
- Memory organization 512 x 32-bit (2 KB)
- Bit program operation
- Data retention: >10 Years
- Access time: 50 ns (max)
- Bit cell program time: 10 us (min)

2.9. System Peripherals

2.9.1. SPI

The SPI of JH7110 has the following features.

- Support 7 SPI interfaces
- Support serial-master and serial-slave mode, software-configurable
- Separate data input and output bit
- Provide configurable FIFO with size up to 8 × 16-bit for both TX and RX channel
- Support DMA access for TX and RX FIFO

2.9.2. UART

The UART of JH7110 has the following features.

- Support 6 UART interfaces
- Support 4-wire mode (HW flow control with CTS/RTS)
- Separate up to 256-Byte of TX and 384-Byte of RX FIFOs
- Programmable FIFO disabling for 1-Byte depth
- Programmable baud rate generator supports up to 3 Mbps
- Support DMA access for TX and RX channel
- Standard asynchronous communication bits (for start, stop, and parity).
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- False start bit detection
- Line break generation and detection
- Programmable hardware flow control
- Fully-programmable serial interface characteristics

Note:
3 Mbps rate is supported by UART3, UART4 and UART5. Use the fraction in SYSTOP_CRG.

2.9.3. I2C

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The I2C of JH7110 has the following features.

- Support 7 I2C interfaces
- Compatible with Philips I2C standard
- Support multi-master operation
- Provide software-programmable clock frequency
- Support clock Stretching and “Wait” state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Support 7-bit and 10-bit addressing modes
- Operates from a wide range of input clock frequencies
- Support 100 KHz/400 KHz/1 MHz modes

2.9.4. Timer

The timer of JH7110 has the following features.

- 4 timers for system application
- Maskable interrupt
- Register lock function
- Programmable output frequency

2.9.5. Watchdog

The watchdog of JH7110 has the following features.

- 32-bit down counter
- Non-Maskable Interrupt (NMI) or WDOG reset
- Optional automatic WDOG reset if NMI handler fails to update the Watchdog register
- Maskable Watchdog freeze by a user program
- Configurable clock source

2.9.6. Temp Sensor

The temperature sensor of JH7110 has the following features.

- ±3 ℃ untrimmed accuracy (-40 ℃ to 100 ℃)
- ±1.0 ℃ trimmed accuracy (0 ℃ to 70 ℃)
- ±1.25 ℃ trimmed accuracy (-40 ℃ to 125 ℃)
- Calibration sequence requires no knowledge of die temperature
- Digital interface, 12-bit resolution

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2.9.7. PLL

The PLL of JH7110 has the following features.

- Dual power supply: 1.8 V (analog)/0.9 V(digital) allows for excellent supply noise rejection
- Reference clock frequency range from 5 MHz to 500 MHz
- PFD frequency range 5 MHz to 100 MHz
- VCO frequency range from 1 GHz to 3 GHz
- Low jitter
- Lock detector to indicate frequency locked state

2.9.8. RTC

The RTC of JH7110 provides the following features.

- Less DFF/Power
- Provide calendar register with year, month, day, hour, minute, second
- Support leap year judgment
- The range is 2001/01/01/00/00/00 to 2099/12/31/23/59/59
- Support DayClk/HourClk/MinClk, in BCD code
- Implement timer interrupt function through register
- The clock frequency of the input crystal is 32768 Hz
- There are 32 reference calibration clocks chosen by software with reference clock coming from GPIO
- Hardware calibration interval is 1D/1H only works when reference calibration clock connected
- Support software calibration

2.9.9. INTC

The INTC of JH7110 has the following features.

- 2 INTCs that support a total 4 sets of 32-bit source interrupt input
- Support separate interrupt with a programmable type (level, edge) and polarity
- Software interrupt control

2.9.10. PWM

The PWM of JH7110 has the following features.

- Support 8 PWM interfaces
- 32-bit counter/timer facility
- Single-run or continuous run of PTC counter
- Programmable PWM mode
- System clock and external clock sources for timer functionality
- HI/LO Reference and Capture registers
- 3-state control for PWM output driver
- PWM/Timer/Counter functionalities can cause an interrupt to the CPU

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2.9.11. GPCLK

The GPCLK of JH7110 has the following features.

- Support 3 general-purpose clock outputs to GPIO pins.
- Output clock up to 50 MHz

2.9.12. Mailbox

The mailbox of JH7110 has the following features.

- Send messages or signals between RISC-V cores
- Support 4 mailbox elements, and each mailbox element includes 1 data word, 1 command register, and 1 flag bit for interrupt
- Provide 32 registers for software to use to indicate whether the mailbox is occupied

2.9.13. GPIO

The GPIO of JH7110 has the following features.

- Support up to 64 GPIOs
- Individually programmable input/output pins, default to output at reset.
- Each GPIO has a dedicated control signal
- Support separate interrupt with a programmable type (level, edge) and polarity
- All pins with MUX with function pins

2.10. Others

JH7110 has the following miscellaneous features.

Boot Devices

JH7110 supports the following boot devices.

- QSPI Flash (For **SPL + OpenSBI + U-Boot**) + NVMe/SD Card/eMMC (For **Kernel + File System** and later)

Note:
System will detect in sequence whether it can boot from the following device sequence: **NVMe > SD > eMMC**. For example, if the boot program is found on the SD, eMMC will be ignored.

Clock Source

Oscillator (OSC):

- OSC 24 MHz system main clock source
- OSC 32.768 KHz for RTC clock source

Package

- Body Size 17 mm x 17 mm, 0.65 mm ball pitch, FCBGA 625 balls

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Power Supply

- 0.9 V core voltage
- 3.3 V/2.5 V/1.8 V I/O voltage

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3. Signal Description

The following table displays the system signals of JH7110, including Pull-Up (PU) and Pull-Down (PD) settings.

Note:
The maximum current that a GPIO pin can afford is 3 A.

Note:
The following table only displays the default Pull-Up and Pull-Down settings of a signal. By writing 0 (No) or 1 (Yes) to the following signals, most of the PU/PD settings are configurable. "Tied to" means the PU PD settings of the signal are fixed, and not configurable.

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Table 3-1 System Signal Description

Signal Name	Description	PU	PD
TESTEN	Test Enable Signal Negative	Tied to 0	Tied to 1
RGPIO0	RGPIO0	0	0
RGPIO1	RGPIO1	0	0
RGPIO2	RGPIO2	0	0
RGPIO3	RGPIO3	0	1
SD_SEL18	SD Select 18	0	1
QSPI_SEL18	QSPI Select 18	1	0
GPIO0	GPIO0	0	0
GPIO1	GPIO1	1	0
GPIO2	GPIO2	0	0
GPIO3	GPIO3	0	0
GPIO4	GPIO4	1	0
GPIO5	GPIO5	1	0
GPIO6	GPIO6	1	0
GPIO7	GPIO7	0	0
GPIO8	GPIO8	0	0
GPIO9	GPIO9	1	0
GPIO10	GPIO10	0	0
GPIO11	GPIO11	0	0
GPIO12	GPIO12	1	0
GPIO13	GPIO13	1	0
GPIO14	GPIO14	0	0
GPIO15	GPIO15	0	0
GPIO16	GPIO16	0	0
GPIO17	GPIO17	0	0
GPIO18	GPIO18	1	0
GPIO19	GPIO19	1	0
GPIO20	GPIO20	0	0
GPIO21	GPIO21	0	0
GPIO22	GPIO22	0	0
GPIO23	GPIO23	0	0
GPIO24	GPIO24	0	0
GPIO25	GPIO25	0	0
GPIO26	GPIO26	0	0

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Table 3-1 System Signal Description (continued)

Signal Name	Description	PU	PD
GPIO27	GPIO27	0	0
GPIO28	GPIO28	0	0
GPIO29	GPIO29	0	0
GPIO30	GPIO30	0	0
GPIO31	GPIO31	0	0
GPIO32	GPIO32	0	0
GPIO33	GPIO33	0	0
GPIO34	GPIO34	0	1
GPIO35	GPIO35	0	0
GPIO36	GPIO36	1	0
GPIO37	GPIO37	1	0
GPIO38	GPIO38	1	0
GPIO39	GPIO39	1	0
GPIO40	GPIO40	1	0
GPIO41	GPIO41	1	0
GPIO42	GPIO42	1	0
GPIO43	GPIO43	1	0
GPIO44	GPIO44	1	0
GPIO45	GPIO45	1	0
GPIO46	GPIO46	1	0
GPIO47	GPIO47	1	0
GPIO48	GPIO48	1	0
GPIO49	GPIO49	0	0
GPIO50	GPIO50	0	0
GPIO51	GPIO51	0	0
GPIO52	GPIO52	1	0
GPIO53	GPIO53	0	0
GPIO54	GPIO54	0	0
GPIO55	GPIO55	0	0
GPIO56	GPIO56	1	0
GPIO57	GPIO57	0	0
GPIO58	GPIO58	0	0
GPIO59	GPIO59	0	0
GPIO60	GPIO60	1	0

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Table 3-1 System Signal Description (continued)

Signal Name	Description	PU	PD
GPIO61	GPIO61	0	0
GPIO62	GPIO62	0	0
GPIO63	GPIO63	0	0
RSTN	Reset Negative	Tied to 1	Tied to 0
RTC_XIN	RTC Input Signal	NONE	NONE
RTC_XOUT	RTC Output Signal	NONE	NONE
OSC_XIN	Oscillator Input Signal	NONE	NONE
OSC_XOUT	Oscillator Output Signal	NONE	NONE
SD0_CLK	SD0 Clock Signal	0	0
SD0_CMD	SD0 Command Signal	0	0
SD0_DATA0	SD0 DATA Lane 0	1	0
SD0_DATA1	SD0 DATA Lane 1	0	0
SD0_DATA2	SD0 DATA Lane 2	0	0
SD0_DATA3	SD0 DATA Lane 3	1	0
SD0_DATA4	SD0 DATA Lane 4	1	0
SD0_DATA5	SD0 DATA Lane 5	0	0
SD0_DATA6	SD0 DATA Lane 6	0	0
SD0_DATA7	SD0 DATA Lane 7	0	0
SD0_STRB	SD0 STR8	0	0
GMAC1_MDC	GMAC1 Management Device Clock	NONE	NONE
GMAC1_MDIO	GMAC1 Management Data Input and Output	NONE	NONE
GMAC1_RXD0	GMAC1 Input Data Lane 0	NONE	NONE
GMAC1_RXD1	GMAC1 Input Data Lane 1	NONE	NONE
GMAC1_RXD2	GMAC1 Input Data Lane 2	NONE	NONE
GMAC1_RXD3	GMAC1 Input Data Lane 3	NONE	NONE
GMAC1_RXDV	GMAC1 Input Collision and Data Valid	NONE	NONE
GMAC1_RXC	GMAC1 Input Clock	NONE	NONE
GMAC1_TXD0	GMAC1 Output Data Lane 0	NONE	NONE
GMAC1_TXD1	GMAC1 Output Data Lane 1	NONE	NONE
GMAC1_TXD2	GMAC1 Output Data Lane 2	NONE	NONE
GMAC1_TXD3	GMAC1 Output Data Lane 3	NONE	NONE
GMAC1_TXEN	GMAC1 Output Enable	NONE	NONE
GMAC1_TXC	GMAC1 Output Clock	NONE	NONE
GMAC0_MDC	GMAC0 Management Device Clock	NONE	NONE

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Table 3-1 System Signal Description (continued)

Signal Name	Description	PU	PD
GMAC0_MDIO	GMAC0 Management Data Input and Output	NONE	NONE
GMAC0_RXD0	GMAC0 Input Data Lane 0	NONE	NONE
GMAC0_RXD1	GMAC0 Input Data Lane 1	NONE	NONE
GMAC0_RXD2	GMAC0 Input Data Lane 2	NONE	NONE
GMAC0_RXD3	GMAC0 Input Data Lane 3	NONE	NONE
GMAC0_RXDV	GMAC0 Input Collision and Data Valid	NONE	NONE
GMAC0_RXC	GMAC0 Input Clock	NONE	NONE
GMAC0_TXD0	GMAC0 Output Data Lane 0	NONE	NONE
GMAC0_TXD1	GMAC0 Output Data Lane 1	NONE	NONE
GMAC0_TXD2	GMAC0 Output Data Lane 2	NONE	NONE
GMAC0_TXD3	GMAC0 Output Data Lane 3	NONE	NONE
GMAC0_TXEN	GMAC0 Output Enable	NONE	NONE
GMAC0_TXC	GMAC0 Output Clock	NONE	NONE
QSPI_SCLK	QSPI_SCLK	0	0
QSPI_CSn0	QSPI Chip Select	1	0
QSPI_DATA0	QSPI Data Lane 0	0	0
QSPI_DATA1	QSPI Data Lane 1	0	0
QSPI_DATA2	QSPI Data Lane 2	0	0
QSPI_DATA3	QSPI Data lane 3	0	0
OTP_PENVDD2	OTP_PENVDD2	NONE	NONE
DDR_ACT_N	DDR_ACT_N	NONE	NONE
DDR_ADR[13:0]	DDR Address [13:0]	NONE	NONE
DDR_ATB0	DDR_ATB0	NONE	NONE
DDR_ATB1	DDR_ATB1	NONE	NONE
DDR_BA[1:0]	DDR BANK Address Input [1:0]	NONE	NONE
DDR_BG[1:0]	DDR_BG[1:0]	NONE	NONE
DDR_CAL	DDR_CAL	NONE	NONE
DDR_CAS_N_ADR15	DDR Column Address Select Address 15	NONE	NONE
DDR_CKE[1:0]	DDR Clock Enable [1:0]	NONE	NONE
DDR_CK_N[1:0]	DDR Clock Negative [1:0]	NONE	NONE
DDR_CK_P[1:0]	DDR Clock Positive [1:0]	NONE	NONE
DDR_CS_N[3:0]	DDR Chip Select Negative [3:0]	NONE	NONE
DDR_DM_DBI_N[3:0]	DDR_DM_DBI_N[3:0]	NONE	NONE
DDR_DQ[0:31]	DDR Data Communication [0:31]	NONE	NONE

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Table 3-1 System Signal Description (continued)

Signal Name	Description	PU	PD
DDR_DQS_N[3:0]	DDR Data Communication Select Negative [3:0]	NONE	NONE
DDR_DQS_P[3:0]	DDR Data Communication Select Positive [3:0]	NONE	NONE
DDR_ERR_N	DDR Error Negative	NONE	NONE
DDR_ODT[1:0]	DDR On-Die Termination [1:0]	NONE	NONE
DDR_PAR	DDR_PAR	NONE	NONE
DDR_PLL_REFOUT_N	DDR PLL Reference Output Negative	NONE	NONE
DDR_PLL_REFOUT_P	DDR PLL Reference Output Positive	NONE	NONE
DDR_PLL_TESTOUT_N	DDR PLL Test Output Negative	NONE	NONE
DDR_PLL_TESTOUT_P	DDR PLL Test Output Positive	NONE	NONE
DDR_RAS_N_ADR16	DDR Row Address Select Negative Address 16	NONE	NONE
DDR_RESET_N	DDR Reset Negative	NONE	NONE
DDR_WE_N_ADR14	DDR Write Enable Negative Address 14	NONE	NONE
HDMITX0_EXTR	HDMI Output 0 Extra	NONE	NONE
HDMITX0_TX0N	HDMI Output 0 Negative	NONE	NONE
HDMITX0_TX0P	HDMI Output 0 Positive	NONE	NONE
HDMITX0_TX1N	HDMI Output 1 Negative	NONE	NONE
HDMITX0_TX1P	HDMI Output 1 Positive	NONE	NONE
HDMITX0_TX2N	HDMI Output 2 Negative	NONE	NONE
HDMITX0_TX2P	HDMI Output 2 Positive	NONE	NONE
HDMITX0_TX3N	HDMI Output 3 Negative	NONE	NONE
HDMITX0_TX3P	HDMI Output 3 Positive	NONE	NONE
MIPITX_L0N	MIPI Output Lane 0 Negative	NONE	NONE
MIPITX_L0P	MIPI Output Lane 0 Positive	NONE	NONE
MIPITX_L1N	MIPI Output Lane 1 Negative	NONE	NONE
MIPITX_L1P	MIPI Output Lane 1 Positive	NONE	NONE
MIPITX_L2N	MIPI Output Lane 2 Negative	NONE	NONE
MIPITX_L2P	MIPI Output Lane 2 Positive	NONE	NONE
MIPITX_L3N	MIPI Output Lane 3 Negative	NONE	NONE
MIPITX_L3P	MIPI Output Lane 3 Positive	NONE	NONE
MIPITX_L4N	MIPI Output Lane 4 Negative	NONE	NONE
MIPITX_L4P	MIPI Output Lane 4 Positive	NONE	NONE
MIPIRX_DN0	MIPI Input DN Lane 0	NONE	NONE
MIPIRX_DN1	MIPI Input DN Lane 1	NONE	NONE
MIPIRX_DN2	MIPI Input DN Lane 2	NONE	NONE

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Table 3-1 System Signal Description (continued)

Signal Name	Description	PU	PD
MIPIRX_DN3	MIPI Input DN Lane 3	NONE	NONE
MIPIRX_DN4	MIPI Input DN Lane 4	NONE	NONE
MIPIRX_DN5	MIPI Input DN Lane 5	NONE	NONE
MIPIRX_DP0	MIPI Input DP Lane 0	NONE	NONE
MIPIRX_DP1	MIPI Input DP Lane 1	NONE	NONE
MIPIRX_DP2	MIPI Input DP Lane 2	NONE	NONE
MIPIRX_DP3	MIPI Input DP Lane 3	NONE	NONE
MIPIRX_DP4	MIPI Input DP Lane 4	NONE	NONE
MIPIRX_DP5	MIPI Input DP Lane 5	NONE	NONE
PCIE0_CKREFN	PCIE0 Clock Reference Negative	NONE	NONE
PCIE0_CKREFP	PCIE0 Clock Reference Positive	NONE	NONE
PCIE0_RXN	PCIE0 Input Negative	NONE	NONE
PCIE0_RXP	PCIE0 Input Positive	NONE	NONE
PCIE0_TXN	PCIE0 Output Negative	NONE	NONE
PCIE0_TXP	PCIE0 Output Positive	NONE	NONE
PCIE1_CKREFN	PCIE1 Clock Reference Negative	NONE	NONE
PCIE1_CKREFP	PCIE1 Clock Reference Positive	NONE	NONE
PCIE1_RXN	PCIE1 Input Negative	NONE	NONE
PCIE1_RXP	PCIE1 Input Positive	NONE	NONE
PCIE1_TXN	PCIE1 Output Negative	NONE	NONE
PCIE1_TXP	PCIE1 Output Positive	NONE	NONE
USB_DM	USB Device Management	NONE	NONE
USB_DP	USB DP	NONE	NONE
USB_ID	USB ID	NONE	NONE
USB_RREF	USB_RREF	NONE	NONE
USB_VBUS	USB_VBUS	NONE	NONE
ANA18_TEMP_VCAL	Analog 18 Temperature VCAL	NONE	NONE
ANA18_TEMP_VSS	Analog 18 Temperature VSS	NONE	NONE
ANA18_TEMP_TEST1	Analog 18 Temperature Test 1	NONE	NONE
ANA18_TEMP_TEST0	Analog 18 Temperature Test 0	NONE	NONE

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3.1. Pin Map

The following figure provides a general view of the pins and their corresponding signal names, for more detailed information, see Pin List *(on page 43)*.

In the figure, a letter on the left edge from “A” to “AE” and a number on the top edge from “1” to “25” are used together to indicate a pin location. For example, A1 = “VSS”, A2 = “QSPI_DATA0”, and so forth.

Figure 3-1 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	VSS	QSPI_DATA0	QSPI_SCLK	GPIO0	AVSS_PCIE1	PCIE1_CKREFN	AVSS_PCIE1	PCIE1_TXP	AVSS_PCIE0	PCIE0_CKREFN	AVSS_PCIE0	PCIE0_TXP	AVSS_PCIE0	USB_ID	USB_DP	USB_DM	GPIO49	GPIO53	GPIO51	AVSS_HDMI	HDMITX0_TX2P	HDMITX0_TX2N	HDMITX0_TX1P	HDMITX0_TX1N	AVSS_HDMI
B	QSPI_DATA2	QSPI_DATA1	QSPI_CSN0	GPIO2	AVSS_PCIE1	PCIE1_CKREFP	AVSS_PCIE1	PCIE1_TXN	AVSS_PCIE1	PCIE0_CKREFP	AVSS_PCIE0	PCIE0_TXN	AVSS_PCIE0	USB_VBUS18	VCCA33_USB	AVSS_USB	VSS	GPIO52	GPIO41	GPIO42	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI
C	QSPI_DATA3	VSS	PAD_QSPI_SEL18	GPIO1	GPIO3	GPIO4	PCIE1_RXP	AVSS_PCIE1	AVDL_PCIE1	AVSS_PCIE0	PCIE0_RXP	AVDL_PCIE0	AVSS_PCIE0	USB_RREF	VCCA18_USB	AVSS_USB	GPIO45	VSS	GPIO39	VSS	GPIO59	AVDD09_HDMI	AVDD_HDMI	HDMITX0_TX0P	HDMITX0_TX0N
D	SD0_DATA0	SD0_CLK	VDD1833_QSPI	VSS	GPIO6	GPIO5	PCIE1_RXN	AVSS_PCIE1	AVDH_PCIE1	AVSS_PCIE0	PCIE0_RXN	AVSS_PCIE0	AVSS_PCIE0	AVDD09_USB	GPIO50	GPIO56	GPIO62	GPIO37	VSS	GPIO63	GPIO36	AVDD_HDMI	AVSS_HDMI	AVSS_HDMI	HDMITX0_TX3P
E	SD0_DATA1	SD0_DATA3	VSS	SD0_CMD	SD0_DATA2	PAD_SD_SEL18	VSS	VDD1833_GPIO3	VSS	VSS	AVSS_PCIE0	VSS	AVDH_PCIE0	AVSS_USB	GPIO54	GPIO48	VSS	GPIO46	GPIO55	VSS	GPIO43	PVSS_HDMI	PVDD_HDMI	HDMITX0_EXTR	HDMITX0_TX3N
F	GPIO18	GPIO16	SD0_DATA4	SD0_DATA5	SD0_DATA7	SD0_DATA6	SD0_STRB	VSS	VDD1833_SD0	VSS	VSS	VSS	VSS	GPIO47	VDD1833_GPIO2	VDD1833_GPIO2	GPIO38	GPIO40	GPIO60	GPIO61	GPIO57	GPIO44	VSS	VSS	AVSS_HDMI
G	GPIO17	VSS	GPIO15	GPIO14	GPIO20	GPIO19	VSS	VSS	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	GPIO58	VSS	VSS	MIPITX_L0N	MIPITX_L0P
H	GPIO9	GPIO11	GPIO13	VSS	GPIO12	VDD1833_GPIO4	VSS	VDD	VDD	VSS	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	MIPITX_L1N	MIPITX_L1P
J	GPIO8	VSS	GPIO7	GPIO10	VSS	VDD	VDD	VSS	VSS	VSS	VDD_CPU	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VSS	MIPITX_L2N	MIPITX_L2P
K	GMAC1_TXD3	GMAC1_TXC	GMAC1_RXDV	GMAC1_TXD2	GMAC1_TXEN	VSS	VDD	VSS	VSS	VDD_CPU	VSS	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VDD_MIPITX	MIPITX_L3N	MIPITX_L3P
L	GMAC1_TXD0	VSS	GMAC1_RXD0	VSS	VSS	VSS	VDD	VDD	VSS	VDD_CPU	VSS	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VDD	VDD	VSS	VDD	VSS	VCC18A_MIPITX	VSS	MIPITX_L4N	MIPITX_L4P
M	GMAC1_RXD1	GMAC1_MDIO	GMAC1_RXC	GMAC1_TXD1	VDD1825_GMAC1	VSS	VSS	VDD	VSS	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	VSS	VSS	VSS	VSS	VDD	VSS	VSS	VSS	VSS	GND09A_MIPIRX	MIPIRX_DN5	MIPIRX_DP5
N	GMAC1_MDC	GMAC1_RXD3	GMAC1_RXD2	VDD1825_GMAC0	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VCC18A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN4	MIPIRX_DP4
P	GMAC0_TXEN	VSS	GMAC0_TXD2	VSS	OTP_PENVDD2	VSS18_OTP	VDD18_OTP	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VDD	VSS	VDD	VSS	VDDA18_TEMP	VSS	VSS	VCC09A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN3	MIPIRX_DP3
R	GMAC0_TXD1	GMAC0_TXC	VSS	GMAC0_RXD1	VCCA18_PLL0	VCCA18_PLL2	VCCA18_PLL1	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS18_TEMP	ANA18_TEMP_VSS	ANA18_TEMP_TEST1	GND09A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN2	MIPIRX_DP2
T	GMAC0_RXDV	GMAC0_RXC	GMAC0_TXD3	VSS	VSS_PLL0	VSS_PLL2	VSS_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDPLL_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VDD18_TEMP	ANA18_TEMP_VCAL	ANA18_TEMP_TEST0	GPIO35	GND09A_MIPIRX	MIPIRX_DN1	MIPIRX_DP1
U	VSS	GMAC0_RXD2	GMAC0_RXD0	GMAC0_TXD0	VDD_PLL0	VDD_PLL2	VDD_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VSS	VDD1833_GPIO1	GPIO34	GPIO33	GND09A_MIPIRX	MIPIRX_DN0	MIPIRX_DP0
V	RSTN	GMAC0_MDC	GMAC0_RXD3	GMAC0_MDIO	VSS_PLL0	VSS_PLL2	VSS_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VSS	VDD1833_GPIO1	VSS	GPIO32	VSS	GPIO28	GND09A_MIPIRX	GND09A_MIPIRX
W	TESTEN	RGPIO2	VSS	RGPIO0	RGPIO1	RGPIO3	VSS	VDD_DDR	VDD_DDR	VSS	VSS	VSS	VSS	VDDQCK_DDR	VSS	VSS	VSS	VSS	GPIO29	GPIO31	GPIO27	GPIO24	GPIO26	GPIO21	GPIO25
Y	RTC_XIN	RTC_XOUT	VDD_RTC	VSS	VDD1833_AON	VSS	VDD_DDR	VDD_DDR	VSS	VSS	VSS	DDR_ADR[5]	DDR_BG[1]	VSS	DDR_PLL_REFOUT_N	DDR_CKE[1]	DDR_PLL_TESTOUT_P	VSS	VSS	GPIO30	GPIO22	VSS	GPIO23	VSS	DDR_DQ[3]
AA	VSS_RTC	VSS18_OSC	VDD18_OSC	VSS	VSS	VSS	VDD_DDR	VSS	VSS	DDR_ADR[13]	DDR_ADR[6]	DDR_ADR[7]	DDR_BA[1]	DDR_CS_N[3]	DDR_PLL_REFOUT_P	VSS	DDR_PLL_TESTOUT_N	DDR_CKE[0]	VSS	VSS	DDR_DQ[9]	DDR_DQ[13]	DDR_DQ[7]	DDR_DQ[6]	DDR_DM_DBI_N[0]
AB	OSC_XIN	OSC_XOUT	VSS	DDR_DQ[28]	DDR_DQ[31]	VSS	VSS	DDR_DQ[23]	DDR_DQ[20]	VSS	DDR_ADR[0]	DDR_ACT_N	VSS	DDR_RAS_N_ADR16	DDR_CAS_N_ADR15	DDR_BA[0]	DDR_CS_N[1]	DDR_RESET_N	VSS	DDR_DQ[12]	DDR_DQ[11]	VSS	DDR_DQ[2]	VSS	DDR_DQ[0]
AC	VSS	VSS	DDR_DQ[29]	VSS	DDR_DQ[30]	VSS	DDR_DQ[22]	VSS	DDR_DQ[18]	DDR_ADR[12]	DDR_ADR[11]	DDR_ADR[8]	DDR_ADR[2]	DDR_ADR[1]	DDR_BG[0]	DDR_ATB1	VSS	DDR_CS_N[0]	DDR_ODT[0]	DDR_DQ[15]	VSS	DDR_DQ[10]	VSS	DDR_DQ[4]	DDR_DQ[1]
AD	DDR_DM_DBI_N[3]	DDR_DQ[27]	DDR_DQ[25]	DDR_DQS_N[3]	VSS	DDR_DQ[21]	DDR_DQS_N[2]	DDR_DQ[19]	DDR_DQ[17]	VSS	DDR_ADR[10]	DDR_CK_P[1]	DDR_ADR[3]	VSS	DDR_CK_N[0]	DDR_ERR_N	DDR_ATB0	DDR_CS_N[2]	DDR_ODT[1]	DDR_DQ[14]	DDR_DQ[8]	DDR_DQS_P[1]	DDR_DQ[5]	DDR_DQS_N[0]	VSS
AE	VSS	VSS	DDR_DQ[24]	DDR_DQS_P[3]	DDR_DQ[26]	DDR_DM_DBI_N[2]	DDR_DQS_P[2]	VSS	DDR_DQ[16]	DDR_ADR[9]	DDR_ADR[4]	DDR_CK_N[1]	VSS	DDR_PAR	DDR_CK_P[0]	VSS	DDR_WE_N_ADR1	VSS	DDR_CAL	DDR_DM_DBI_N[1]	VSS	DDR_DQS_N[1]	VSS	DDR_DQS_P[0]	VSS

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3.2. Pin List

The following table shows the signal names for each pin.

Table 3-2 Pin List Description (A)

Pin No.	Signal Name
A1	VSS
A2	QSPI_DATA0
A3	QSPI_SCLK
A4	GPIO0
A5	AVSS_PCIE1
A6	PCIE1_CKREFN
A7	AVSS_PCIE1
A8	PCIE1_TXP
A9	AVSS_PCIE0
A10	PCIE0_CKREFN
A11	AVSS_PCIE0
A12	PCIE0_TXP
A13	AVSS_PCIE0
A14	USB_ID
A15	USB_DP
A16	USB_DM
A17	GPIO49
A18	GPIO53
A19	GPIO51
A20	AVSS_HDMI
A21	HDMITX0_TX2P
A22	HDMITX0_TX2N
A23	HDMITX0_TX1P
A24	HDMITX0_TX1N
A25	AVSS_HDMI

Table 3-3 Pin List Description (B)

Pin No.	Signal Name
B1	QSPI_DATA2
B2	QSPI_DATA1
B3	QSPI_CSN0
B4	GPIO2
B5	AVSS_PCIE1
B6	PCIE1_CKREFP
B7	AVSS_PCIE1
B8	PCIE1_TXN
B9	AVSS_PCIE1
B10	PCIE0_CKREFP
B11	AVSS_PCIE0
B12	PCIE0_TXN
B13	AVSS_PCIE0
B14	USB_VBUS18
B15	VCCA33_USB
B16	AVSS_USB
B17	VSS
B18	GPIO52
B19	GPIO41
B20	GPIO42
B21	AVSS_HDMI
B22	AVSS_HDMI
B23	AVSS_HDMI
B24	AVSS_HDMI
B25	AVSS_HDMI

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Table 3-4 Pin List Description (C)

Pin No.	Signal Name
C1	QSPI_DATA3
C2	VSS
C3	QSPI_SEL18
C4	GPIO1
C5	GPIO3
C6	GPIO4
C7	PCIE1_RXP
C8	AVSS_PCIE1
C9	AVDL_PCIE1
C10	AVSS_PCIE0
C11	PCIE0_RXP
C12	AVDL_PCIE0
C13	AVSS_PCIE0
C14	USB_RREF
C15	VCCA18_USB
C16	AVSS_USB
C17	GPIO45
C18	VSS
C19	GPIO39
C20	VSS
C21	GPIO59
C22	AVDD09_HDMI
C23	AVDD_HDMI
C24	HDMITX0_TX0P
C25	HDMITX0_TX0N

Table 3-5 Pin List Description (D)

Pin No.	Signal Name
D1	SD0_DATA0
D2	SD0_CLK
D3	VDD1833_QSPI
D4	VSS
D5	GPIO6
D6	GPIO5
D7	PCIE1_RXN
D8	AVSS_PCIE1
D9	AVDH_PCIE1
D10	AVSS_PCIE0
D11	PCIE0_RXN
D12	AVSS_PCIE0
D13	AVSS_PCIE0
D14	AVDD09_USB
D15	GPIO50
D16	GPIO56
D17	GPIO62
D18	GPIO37
D19	VSS
D20	GPIO63
D21	GPIO36
D22	AVDD_HDMI
D23	AVSS_HDMI
D24	AVSS_HDMI
D25	HDMITX0_TX3P

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Table 3-6 Pin List Description (E)

Pin No.	Signal Name
E1	SD0_DATA1
E2	SD0_DATA3
E3	VSS
E4	SD0_CMD
E5	SD0_DATA2
E6	SD_SEL18
E7	VSS
E8	VDD1833_GPIO3
E9	VSS
E10	VSS
E11	AVSS_PCIE0
E12	VSS
E13	AVDH_PCIE0
E14	AVSS_USB
E15	GPIO54
E16	GPIO48
E17	VSS
E18	GPIO46
E19	GPIO55
E20	VSS
E21	GPIO43
E22	PVSS_HDMI
E23	PVDD_HDMI
E24	HDMITX0_EXTR
E25	HDMITX0_TX3N

Table 3-7 Pin List Description (F)

Pin No.	Signal Name
F1	GPIO18
F2	GPIO16
F3	SD0_DATA4
F4	SD0_DATA5
F5	SD0_DATA7
F6	SD0_DATA6
F7	SD0_STRB
F8	VSS
F9	VDD1833_SD0
F10	VSS
F11	VSS
F12	VSS
F13	VSS
F14	GPIO47
F15	VDD1833_GPIO2
F16	VDD1833_GPIO2
F17	GPIO38
F18	GPIO40
F19	GPIO60
F20	GPIO61
F21	GPIO57
F22	GPIO44
F23	VSS
F24	VSS
F25	AVSS_HDMI

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Table 3-8 Pin List Description (G)

Pin No.	Signal Name
G1	GPIO17
G2	VSS
G3	GPIO15
G4	GPIO14
G5	GPIO20
G6	GPIO19
G7	VSS
G8	VSS
G9	VDD
G10	VDD
G11	VDD
G12	VSS
G13	VSS
G14	VSS
G15	VSS
G16	VSS
G17	VSS
G18	VSS
G19	VSS
G20	VSS
G21	GPIO58
G22	VSS
G23	VSS
G24	MIPITX_L0N
G25	MIPITX_L0P

Table 3-9 Pin List Description (H)

Pin No.	Signal Name
H1	GPIO9
H2	GPIO11
H3	GPIO13
H4	VSS
H5	GPIO12
H6	VDD1833_GPIO4
H7	VSS
H8	VDD
H9	VDD
H10	VSS
H11	VDD
H12	VSS
H13	VSS
H14	VSS
H15	VSS
H16	VDD
H17	VDD
H18	VDD
H19	VDD
H20	VDD
H21	VSS
H22	VSS
H23	VSS
H24	MIPITX_L1N
H25	MIPITX_L1P

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Table 3-10 Pin List Description (J)

Pin No.	Signal Name
J1	GPIO8
J2	VSS
J3	GPIO7
J4	GPIO10
J5	VSS
J6	VDD
J7	VDD
J8	VSS
J9	VSS
J10	VSS
J11	VDD_CPU
J12	VDD_CPU
J13	VDD_CPU
J14	VSS
J15	VSS
J16	VDD
J17	VSS
J18	VDD
J19	VSS
J20	VDD
J21	VDD
J22	VSS
J23	VSS
J24	MIPITX_L2N
J25	MIPITX_L2P

Table 3-11 Pin List Description (K)

Pin No.	Signal Name
K1	GMAC1_TXD3
K2	GMAC1_TXC
K3	GMAC1_RXDV
K4	GMAC1_TXD2
K5	GMAC1_TXEN
K6	VSS
K7	VDD
K8	VSS
K9	VSS
K10	VDD_CPU
K11	VSS
K12	VDD_CPU
K13	VDD_CPU
K14	VSS
K15	VSS
K16	VDD
K17	VSS
K18	VDD
K19	VSS
K20	VDD
K21	VDD
K22	VSS
K23	VDD_MIPITX
K24	MIPITX_L3N
K25	MIPITX_L3P

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Table 3-12 Pin List Description (L)

Pin No.	Signal Name
L1	GMAC1_TXD0
L2	VSS
L3	GMAC1_RXD0
L4	VSS
L5	VSS
L6	VSS
L7	VDD
L8	VDD
L9	VSS
L10	VDD_CPU
L11	VSS
L12	VDD_CPU
L13	VDD_CPU
L14	VSS
L15	VSS
L16	VDD
L17	VDD
L18	VDD
L19	VSS
L20	VDD
L21	VSS
L22	VCC18A_MIPITX
L23	VSS
L24	MIPITX_L4N
L25	MIPITX_L4P

Table 3-13 Pin List Description (M)

Pin No.	Signal Name
M1	GMAC1_RXD1
M2	GMAC1_MDIO
M3	GMAC1_RXC
M4	GMAC1_TXD1
M5	VDD1825_GMAC1
M6	VSS
M7	VSS
M8	VDD
M9	VSS
M10	VDD_CPU
M11	VDD_CPU
M12	VDD_CPU
M13	VDD_CPU
M14	VSS
M15	VSS
M16	VSS
M17	VSS
M18	VDD
M19	VSS
M20	VSS
M21	VSS
M22	VSS
M23	GND09A_MIPIRX
M24	MIPIRX_DN5
M25	MIPIRX_DP5

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Table 3-14 Pin List Description (N)

Pin No.	Signal Name
N1	GMAC1_MDC
N2	GMAC1_RXD3
N3	GMAC1_RXD2
N4	VDD1825_GMAC0
N5	VSS
N6	VSS
N7	VSS
N8	VDD
N9	VDD
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VDD
N15	VDD
N16	VDD
N17	VDD
N18	VDD
N19	VSS
N20	VSS
N21	VSS
N22	VCC18A_MIPIRX
N23	GND09A_MIPIRX
N24	MIPIRX_DN4
N25	MIPIRX_DP4

Table 3-15 Pin List Description (P)

Pin No.	Signal Name
P1	GMAC0_TXEN
P2	VSS
P3	GMAC0_TXD2
P4	VSS
P5	OTP_PENVDD2
P6	VSS18_OTP
P7	VDD18_OTP
P8	VSS
P9	VDD
P10	VDD
P11	VDD
P12	VDD
P13	VSS
P14	VDD
P15	VDD
P16	VSS
P17	VDD
P18	VSS
P19	VDDA18_TEMP
P20	VSS
P21	VSS
P22	VCC09A_MIPIRX
P23	GND09A_MIPIRX
P24	MIPIRX_DN3
P25	MIPIRX_DP3

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Table 3-16 Pin List Description (R)

Pin No.	Signal Name
R1	GMAC0_TXD1
R2	GMAC0_TXC
R3	VSS
R4	GMAC0_RXD1
R5	VCCA18_PLL0
R6	VCCA18_PLL2
R7	VCCA18_PLL1
R8	VSS
R9	VDD
R10	VSS
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R17	VSS
R18	VSS
R19	VSS18_TEMP
R20	ANA18_TEMP_VSS
R21	ANA18_TEMP_TEST1
R22	GND09A_MIPIRX
R23	GND09A_MIPIRX
R24	MIPIRX_DN2
R25	MIPIRX_DP2

Table 3-17 Pin List Description (T)

Pin No.	Signal Name
T1	GMAC0_RXDV
T2	GMAC0_RXC
T3	GMAC0_TXD3
T4	VSS
T5	VSS_PLL0
T6	VSS_PLL2
T7	VSS_PLL1
T8	VSS
T9	VDD_DDR
T10	VDD_DDR
T11	VSS
T12	VDDQ_DDR
T13	VDDQ_DDR
T14	VDDPLL_DDR
T15	VDDQ_DDR
T16	VDDQ_DDR
T17	VDDQ_DDR
T18	VSS
T19	VDD18_TEMP
T20	ANA18_TEMP_VCAL
T21	ANA18_TEMP_TEST0
T22	GPIO35
T23	GND09A_MIPIRX
T24	MIPIRX_DN1
T25	MIPIRX_DP1

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Table 3-18 Pin List Description (U)

Pin No.	Signal Name
U1	VSS
U2	GMAC0_RXD2
U3	GMAC0_RXD0
U4	GMAC0_TXD0
U5	VDD_PLL0
U6	VDD_PLL2
U7	VDD_PLL1
U8	VSS
U9	VDD_DDR
U10	VDD_DDR
U11	VSS
U12	VDDQ_DDR
U13	VDDQ_DDR
U14	VDDQ_DDR
U15	VDDQ_DDR
U16	VDDQ_DDR
U17	VDDQ_DDR
U18	VSS
U19	VSS
U20	VDD1833_GPIO1
U21	GPIO34
U22	GPIO33
U23	GND09A_MIPIRX
U24	MIPIRX_DN0
U25	MIPIRX_DP0

Table 3-19 Pin List Description (V)

Pin No.	Signal Name
V1	RSTN
V2	GMAC0_MDC
V3	GMAC0_RXD3
V4	GMAC0_MDIO
V5	VSS_PLL0
V6	VSS_PLL2
V7	VSS_PLL1
V8	VSS
V9	VDD_DDR
V10	VDD_DDR
V11	VSS
V12	VDDQ_DDR
V13	VDDQ_DDR
V14	VDDQ_DDR
V15	VDDQ_DDR
V16	VDDQ_DDR
V17	VSS
V18	VSS
V19	VDD1833_GPIO1
V20	VSS
V21	GPIO32
V22	VSS
V23	GPIO28
V24	GND09A_MIPIRX
V25	GND09A_MIPIRX

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Table 3-20 Pin List Description (W)

Pin No.	Signal Name
W1	TESTEN
W2	RGPIO2
W3	VSS
W4	RGPIO0
W5	RGPIO1
W6	RGPIO3
W7	VSS
W8	VDD_DDR
W9	VDD_DDR
W10	VSS
W11	VSS
W12	VSS
W13	VSS
W14	VDDQCK_DDR
W15	VSS
W16	VSS
W17	VSS
W18	VSS
W19	GPIO29
W20	GPIO31
W21	GPIO27
W22	GPIO24
W23	GPIO26
W24	GPIO21
W25	GPIO25

Table 3-21 Pin List Description (Y)

Pin No.	Signal Name
Y1	RTC_XIN
Y2	RTC_XOUT
Y3	VDD_RTC
Y4	VSS
Y5	VDD1833_AON
Y6	VSS
Y7	VDD_DDR
Y8	VDD_DDR
Y9	VSS
Y10	VSS
Y11	VSS
Y12	DDR_ADR[5]
Y13	DDR_BG[1]
Y14	VSS
Y15	DDR_PLL_REFOUT_N
Y16	DDR_CKE[1]
Y17	DDR_PLL_TESTOUT_P
Y18	VSS
Y19	VSS
Y20	GPIO30
Y21	GPIO22
Y22	VSS
Y23	GPIO23
Y24	VSS
Y25	DDR_DQ[3]

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Table 3-22 Pin List Description (AA)

Pin No.	Signal Name
AA1	VSS_RTC
AA2	VSS18_OSC
AA3	VDD18_OSC
AA4	VSS
AA5	VSS
AA6	VSS
AA7	VDD_DDR
AA8	VSS
AA9	VSS
AA10	DDR_ADR[13]
AA11	DDR_ADR[6]
AA12	DDR_ADR[7]
AA13	DDR_BA[1]
AA14	DDR_CS_N[3]
AA15	DDR_PLL_REFOUT_P
AA16	VSS
AA17	DDR_PLL_TESTOUT_N
AA18	DDR_CKE[0]
AA19	VSS
AA20	VSS
AA21	DDR_DQ[9]
AA22	DDR_DQ[13]
AA23	DDR_DQ[7]
AA24	DDR_DQ[6]
AA25	DDR_DM_DBI_N[0]

Table 3-23 Pin List Description (AB)

Pin No.	Signal Name
AB1	OSC_XIN
AB2	OSC_XOUT
AB3	VSS
AB4	DDR_DQ[28]
AB5	DDR_DQ[31]
AB6	VSS
AB7	VSS
AB8	DDR_DQ[23]
AB9	DDR_DQ[20]
AB10	VSS
AB11	DDR_ADR[0]
AB12	DDR_ACT_N
AB13	VSS
AB14	DDR_RAS_N_ADR16
AB15	DDR_CAS_N_ADR15
AB16	DDR_BA[0]
AB17	DDR_CS_N[1]
AB18	DDR_RESET_N
AB19	VSS
AB20	DDR_DQ[12]
AB21	DDR_DQ[11]
AB22	VSS
AB23	DDR_DQ[2]
AB24	VSS
AB25	DDR_DQ[0]

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Table 3-24 Pin List Description (AC)

Pin No.	Signal Name
AC1	VSS
AC2	VSS
AC3	DDR_DQ[29]
AC4	VSS
AC5	DDR_DQ[30]
AC6	VSS
AC7	DDR_DQ[22]
AC8	VSS
AC9	DDR_DQ[18]
AC10	DDR_ADR[12]
AC11	DDR_ADR[11]
AC12	DDR_ADR[8]
AC13	DDR_ADR[2]
AC14	DDR_ADR[1]
AC15	DDR_BG[0]
AC16	DDR_ATB1
AC17	VSS
AC18	DDR_CS_N[0]
AC19	DDR_ODT[0]
AC20	DDR_DQ[15]
AC21	VSS
AC22	DDR_DQ[10]
AC23	VSS
AC24	DDR_DQ[4]
AC25	DDR_DQ[1]

Table 3-25 Pin List Description (AD)

Pin No.	Signal Name
AD1	DDR_DM_DBI_N[3]
AD2	DDR_DQ[27]
AD3	DDR_DQ[25]
AD4	DDR_DQS_N[3]
AD5	VSS
AD6	DDR_DQ[21]
AD7	DDR_DQS_N[2]
AD8	DDR_DQ[19]
AD9	DDR_DQ[17]
AD10	VSS
AD11	DDR_ADR[10]
AD12	DDR_CK_P[1]
AD13	DDR_ADR[3]
AD14	VSS
AD15	DDR_CK_N[0]
AD16	DDR_ERR_N
AD17	DDR_ATB0
AD18	DDR_CS_N[2]
AD19	DDR_ODT[1]
AD20	DDR_DQ[14]
AD21	DDR_DQ[8]
AD22	DDR_DQS_P[1]
AD23	DDR_DQ[5]
AD24	DDR_DQS_N[0]
AD25	VSS

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Table 3-26 Pin List Description (AE)

Pin No.	Signal Name
AE1	VSS
AE2	VSS
AE3	DDR_DQ[24]
AE4	DDR_DQS_P[3]
AE5	DDR_DQ[26]
AE6	DDR_DM_DBI_N[2]
AE7	DDR_DQS_P[2]
AE8	VSS
AE9	DDR_DQ[16]
AE10	DDR_ADR[9]
AE11	DDR_ADR[4]
AE12	DDR_CK_N[1]
AE13	VSS
AE14	DDR_PAR
AE15	DDR_CK_P[0]
AE16	VSS
AE17	DDR_WE_N_ADR14
AE18	VSS
AE19	DDR_CAL
AE20	DDR_DM_DBI_N[1]
AE21	VSS
AE22	DDR_DQS_N[1]
AE23	VSS
AE24	DDR_DQS_P[0]
AE25	VSS

3.3. Pin Delay

The following table lists the pin delay information for all pins.

Important:
Make sure you have considered the factor of pin delay in your hardware design practice. Calculate the delay in the target of your design, or your design may not be valid!

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Table 3-27 Pin Delay

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
PMUIO (1.8 V only)			
V1	RSTN	8.496	51.696
W1	TESTEN	7.886	47.788
W4	RGPIO0	8.628	52.471
W5	RGPIO1	6.725	40.215
W2	RGPIO2	7.593	45.947
W6	RGPIO3	5.707	33.512
C3	QSPI_SEL18	7.449	45.165
E6	SD_SEL18	4.336	24.966
GPIO (1.8 V/3.3 V)			
A4	GPIO0	7.93	47.619
C4	GPIO1	7.854	47.673
B4	GPIO2	8.011	48.616
C5	GPIO3	7.316	44.167
C6	GPIO4	6.719	40.341
D6	GPIO5	5.891	33.987
D5	GPIO6	6.746	40.527
J3	GPIO7	4.378	25.22
J1	GPIO8	5.349	31.396
H1	GPIO9	5.548	32.685
J4	GPIO10	3.67	20.842
H2	GPIO11	4.686	27.338
H5	GPIO12	3.241	17.871
H3	GPIO13	4.188	24.119
G4	GPIO14	4.121	23.618
G3	GPIO15	4.846	28.381
F2	GPIO16	5.456	32.142
G1	GPIO17	5.469	32.379
F1	GPIO18	6.198	36.986
G6	GPIO19	3.307	18.431
G5	GPIO20	4.856	28.435
W24	GPIO21	5.514	30.77
Y21	GPIO22	3.878	20.27

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
Y23	GPIO23	4.783	27.698
W22	GPIO24	3.682	20.972
W25	GPIO25	5.707	33.94
W23	GPIO26	4.52	26.269
W21	GPIO27	3.515	19.688
V23	GPIO28	4.367	25.228
W19	GPIO29	2.377	12.518
Y20	GPIO30	3.614	20.45
W20	GPIO31	2.933	16.07
V21	GPIO32	3.322	18.539
U22	GPIO33	3.176	17.641
U21	GPIO34	2.959	16.164
T22	GPIO35	3.085	16.968
D21	GPIO36	7.546	45.483
D18	GPIO37	5.637	32.908
F17	GPIO38	4.047	23.272
C19	GPIO39	6.453	37.013
F18	GPIO40	4.904	28.738
B19	GPIO41	6.164	36.188
B20	GPIO42	6.716	40.21
E21	GPIO43	6.797	40.63
F22	GPIO44	7.777	46.706
C17	GPIO45	5.654	33.384
E18	GPIO46	5.411	31.884
F14	GPIO47	3.046	16.781
E16	GPIO48	4.136	23.561
A17	GPIO49	6.418	37.548
D15	GPIO50	4.236	24.267
A19	GPIO51	6.44	38.243
B18	GPIO52	5.835	34.413
A18	GPIO53	6.256	36.867
E15	GPIO54	4.59	25.789
E19	GPIO55	5.865	34.707

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
D16	GPIO56	5.132	30.065
F21	GPIO57	7.606	45.802
G21	GPIO58	6.029	35.567
C21	GPIO59	7.431	44.784
F19	GPIO60	4.167	23.967
F20	GPIO61	5.471	31.926
D17	GPIO62	4.177	23.474
D20	GPIO63	7.114	42.528
QSPI (1.8 V/3.3 V)			
B3	QSPI_CSN0	7.893	47.992
A2	QSPI_DATA0	8.351	50.84
B2	QSPI_DATA1	8.354	50.795
B1	QSPI_DATA2	8.969	54.869
C1	QSPI_DATA3	7.899	47.964
A3	QSPI_SCLK	8.392	49.953
D2	SD0_CLK	7.684	46.662
E4	SD0_CMD	6.206	37.006
D1	SD0_DATA0	7.598	45.868
E1	SD0_DATA1	7.364	44.438
E5	SD0_DATA2	4.381	25.22
E2	SD0_DATA3	6.795	40.918
F3	SD0_DATA4	6.654	39.921
F4	SD0_DATA5	5.819	34.609
F6	SD0_DATA6	4.716	27.564
F5	SD0_DATA7	4.976	29.278
F7	SD0_STRB	3.129	17.414
GMAC0 (AON 1.8 V/2.5 V)			
V2	GMAC0_MDC	7.183	43.285
V4	GMAC0_MDIO	7.015	42.191
T2	GMAC0_RXC	6.141	36.341
U3	GMAC0_RXD0	6.274	37.566
R4	GMAC0_RXD1	5.31	31.379
U2	GMAC0_RXD2	7.008	41.742

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
V3	GMAC0_RXD3	7.039	42.44
T1	GMAC0_RXDV	6.69	39.723
R2	GMAC0_TXC	5.534	32.54
U4	GMAC0_TXD0	7.188	43.365
R1	GMAC0_TXD1	6.668	39.787
P3	GMAC0_TXD2	6.014	35.675
T3	GMAC0_TXD3	6.194	36.989
P1	GMAC0_TXEN	6.197	36.613
GMAC1 (1.8 V/2.5 V)			
N1	GMAC1_MDC	5.553	32.49
M2	GMAC1_MDIO	4.677	27.191
M3	GMAC1_RXC	4.341	25.117
L3	GMAC1_RXD0	3.828	21.885
M1	GMAC1_RXD1	5.237	30.59
N3	GMAC1_RXD2	5.143	30.176
N2	GMAC1_RXD3	5.406	31.993
K3	GMAC1_RXDV	4.193	24.057
K2	GMAC1_TXC	5.047	29.491
L1	GMAC1_TXD0	5.178	30.475
M4	GMAC1_TXD1	4.716	27.63
K4	GMAC1_TXD2	3.535	19.881
K1	GMAC1_TXD3	5.136	30.248
K5	GMAC1_TXEN	2.751	14.807
MIPI RX			
U24	MIPIRX_DN0	5.802	33.128
T24	MIPIRX_DN1	5.524	32.797
R24	MIPIRX_DN2	5.341	30.292
P24	MIPIRX_DN3	5.343	31.596
N24	MIPIRX_DN4	5.493	31.184
M24	MIPIRX_DN5	5.71	34.001
U25	MIPIRX_DP0	5.788	33.084
T25	MIPIRX_DP1	5.539	32.888
R25	MIPIRX_DP2	5.327	30.147

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
P25	MIPIRX_DP3	5.326	31.503
N25	MIPIRX_DP4	5.479	31.121
M25	MIPIRX_DP5	5.716	32.862
MIPI TX			
G24	MIPITX_L0N	6.669	38.47
G25	MIPITX_L0P	6.657	38.385
H24	MIPITX_L1N	6.403	38.437
H25	MIPITX_L1P	6.369	38.234
J24	MIPITX_L2N	6.261	35.922
J25	MIPITX_L2P	6.237	35.826
K24	MIPITX_L3N	6.039	36.047
K25	MIPITX_L3P	6.047	36.17
L24	MIPITX_L4N	5.891	33.673
L25	MIPITX_L4P	5.872	33.596
HDMI2.0 TX			
E24	HDMITX0_EXTR	6.211	37.205
C25	HDMITX0_TX0N	8.193	49.881
C24	HDMITX0_TX0P	8.176	49.856
A24	HDMITX0_TX1N	8.274	48.233
A23	HDMITX0_TX1P	8.254	48.124
A22	HDMITX0_TX2N	7.43	45.026
A21	HDMITX0_TX2P	7.416	44.923
E25	HDMITX0_TX3N/CKN	7.172	41.445
D25	HDMITX0_TX3P/CKP	7.186	41.576
PCIE2.0 & USB3.0			
A10	PCIE0_CKREFN	6.529	39.089
B10	PCIE0_CKREFP	6.526	39.16
D11	PCIE0_RXN	5.269	31.099
C11	PCIE0_RXP	5.249	30.652
B12	PCIE0_TXN	6.654	40.019
A12	PCIE0_TXP	6.607	39.787
A6	PCIE1_CKREFN	8.065	49.052
B6	PCIE1_CKREFP	8.062	49.07

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
D7	PCIE1_RXN	5.415	31.96
C7	PCIE1_RXP	5.401	31.984
B8	PCIE1_TXN	6.789	40.899
A8	PCIE1_TXP	6.75	40.69
USB2.0			
A16	USB_DM	6.439	38.588
A15	USB_DP	6.447	38.714
A14	USB_ID	5.796	34.529
C14	USB_RREF	5.651	33.469
B14	USB_VBUS18	5.81	34.392
Temp Sensor			
T21	ANA18_TEMP_TEST0	2.714	14.703
R21	ANA18_TEMP_TEST1	2.923	15.951
T20	ANA18_TEMP_VCAL		
R20	ANA18_TEMP_VSS		
System Clock			
AB1	OSC_XIN	8.134	49.408
AB2	OSC_XOUT	7.864	47.685
OTP			
P5	OTP_PENVDD2	2.326	11.787
RTC Clock			
Y1	RTC_XIN	7.972	48.404
Y2	RTC_XOUT	8.091	48.744
DDR			
AB12	DDR_ACT_N	3.668	20.7
AB11	DDR_ADR[0]	4.891	28.586
AC14	DDR_ADR[1]	5.039	29.428
AC13	DDR_ADR[2]	4.521	26.17
AD13	DDR_ADR[3]	5.438	31.998
AE11	DDR_ADR[4]	6.189	37.05
Y12	DDR_ADR[5]	2.949	16.173
AA11	DDR_ADR[6]	3.306	18.373
AA12	DDR_ADR[7]	3.382	18.801

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
AC12	DDR_ADR[8]	4.508	25.888
AE10	DDR_ADR[9]	6.73	40.416
AD11	DDR_ADR[10]	5.196	30.491
AC11	DDR_ADR[11]	4.697	27.161
AC10	DDR_ADR[12]	4.988	29.246
AA10	DDR_ADR[13]	3.888	22.19
AD17	DDR_ATB0	5.631	33.173
AC16	DDR_ATB1	4.854	28.169
AB16	DDR_BA[0]	4.412	25.456
AA13	DDR_BA[1]	3.105	17.126
AC15	DDR_BG[0]	4.882	28.543
Y13	DDR_BG[1]	4.242	24.483
AE19	DDR_CAL	7.062	42.511
AB15	DDR_CAS_N_ADR15	4.126	23.777
AD15	DDR_CK_N[0]	6.764	40.646
AE12	DDR_CK_N[1]	6.339	37.874
AE15	DDR_CK_P[0]	6.765	40.642
AD12	DDR_CK_P[1]	6.337	37.92
AA18	DDR_CKE[0]	5.702	33.81
Y16	DDR_CKE[1]	4.237	24.463
AC18	DDR_CS_N[0]	5.493	32.378
AB17	DDR_CS_N[1]	4.38	25.321
AD18	DDR_CS_N[2]	5.898	34.875
AA14	DDR_CS_N[3]	4.18	23.981
AA25	DDR_DM_DBI_N[0]	7.602	45.995
AE20	DDR_DM_DBI_N[1]	6.988	41.968
AE6	DDR_DM_DBI_N[2]	7.25	43.725
AD1	DDR_DM_DBI_N[3]	9.002	54.835
AB25	DDR_DQ[0]	7.533	45.563
AC25	DDR_DQ[1]	7.483	45.233
AB23	DDR_DQ[2]	6.544	39.104
Y25	DDR_DQ[3]	7.273	43.875
AC24	DDR_DQ[4]	7.957	48.285

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
AD23	DDR_DQ[5]	7.048	42.503
AA24	DDR_DQ[6]	7.68	46.493
AA23	DDR_DQ[7]	6.299	37.554
AD21	DDR_DQ[8]	6.437	38.359
AA21	DDR_DQ[9]	5.74	34.144
AC22	DDR_DQ[10]	6.743	40.499
AB21	DDR_DQ[11]	7.476	45.172
AB20	DDR_DQ[12]	5.962	35.527
AA22	DDR_DQ[13]	6.222	37.214
AD20	DDR_DQ[14]	6.245	37.36
AC20	DDR_DQ[15]	6.046	36.068
AE9	DDR_DQ[16]	6.488	38.961
AD9	DDR_DQ[17]	5.986	35.586
AC9	DDR_DQ[18]	5.001	29.342
AD8	DDR_DQ[19]	6.125	36.548
AB9	DDR_DQ[20]	5.29	31.216
AD6	DDR_DQ[21]	6.794	40.654
AC7	DDR_DQ[22]	5.781	34.332
AB8	DDR_DQ[23]	6.088	36.357
AE3	DDR_DQ[24]	7.907	47.875
AD3	DDR_DQ[25]	8.157	49.547
AE5	DDR_DQ[26]	7.341	44.447
AD2	DDR_DQ[27]	8.194	49.737
AB4	DDR_DQ[28]	7.013	42.311
AC3	DDR_DQ[29]	7.228	43.692
AC5	DDR_DQ[30]	5.989	35.578
AB5	DDR_DQ[31]	5.699	33.823
AD24	DDR_DQS_N[0]	8.248	50.038
AE22	DDR_DQS_N[1]	7.655	46.377
AD7	DDR_DQS_N[2]	7.457	45.17
AD4	DDR_DQS_N[3]	7.84	47.638
AE24	DDR_DQS_P[0]	8.253	50.212
AD22	DDR_DQS_P[1]	7.633	46.2

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Table 3-27 Pin Delay (continued)

Pin	Pin Name	Pin Delay	
		Length (mm)	Delay (ps)
AE7	DDR_DQS_P[2]	7.455	45.16
AE4	DDR_DQS_P[3]	7.83	47.587
AD16	DDR_ERR_N	5.174	30.305
AC19	DDR_ODT[0]	5.876	34.936
AD19	DDR_ODT[1]	6.318	37.747
AE14	DDR_PAR	5.848	34.648
Y15	DDR_PLL_REFOUT_N	3.765	20.351
AA15	DDR_PLL_REFOUT_P	3.767	21.432
AA17	DDR_PLL_TESTOUT_N	3.75	21.23
Y17	DDR_PLL_TESTOUT_P	3.744	21.192
AB14	DDR_RAS_N_ADR16	3.996	22.761
AB18	DDR_RESET_N	4.535	26.169
AE17	DDR_WE_N_ADR14	6.595	39.414

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4. GPIO Functions

JH7110 provides full multiplexing functions to significantly reduce GPIO pins and complexity.

4.1. Function Description

The following table lists the full multiplexing functions of the IO pins.

Important:
JH7110 GPIO supports full multiplexing. This means that a GPIO pin can be configured to any function listed from Function 1 to Function 2 in the following table.

Important:
Function 0 is the default function of an IO. The columns from Function 1 to Function 2 are just used to categorize example functions, you can configure any of the following function to an IO.

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Table 4-1 GPIO Function Description

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO0	SYS_GPIO0	The test reset input line for JTAG, Negative	LCD_CLK	LCD clock	DVP_CLK	DVP clock
GPIO1	SYS_GPIO1	The test clock input line for JTAG	LCD_VSYNC	LCD vertical synchronization	DVP_VSYNC	DVP vertical synchronization
GPIO2	SYS_GPIO2	The *Test Data Input (TDI)* line for JTAG certification	LCD_HSYNC	LCD horizontal synchronization	DVP_HSYNC	DVP horizontal synchronization
GPIO3	SYS_GPIO3	The *Test Data Output (TDO)* line for JTAG certification	LCD_DE	LCD *Data Enable (DE)* mode	DVP_DATA[0]	DVP data lane
GPIO4	SYS_GPIO4	The *Test Mode Selection (TMS)* line for JTAG certification	LCD_-DATAOUT[0]	LCD data output	DVP_DATA[1]	DVP data lane
GPIO5	SYS_GPIO5	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[1]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO6	SYS_GPIO6	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[2]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO7	SYS_GPIO7	GPIO7	LCD_-DATAOUT[3]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO8	SYS_GPIO8	GPIO8	LCD_-DATAOUT[4]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO9	SYS_GPIO9	The test clock input line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[5]	LCD data output	DVP_DATA[6]	DVP data lane
GPIO10	SYS_GPIO10	The *Test Data Input (TDI)* line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[6]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO11	SYS_GPIO11	The *Test Data Output (TDO)* line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[7]	LCD data output	DVP_DATA[8]	DVP data lane
GPIO12	SYS_GPIO12	The *Test Mode Selection (TMS)* line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[8]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO13	SYS_GPIO13	The test reset input line for JTAG on HIFI4 (Audio DSP), Negative	LCD_-DATAOUT[9]	LCD data output	DVP_DATA[10]	DVP data lane
GPIO14	SYS_GPIO14	GPIO14	LCD_-DATAOUT[10]	LCD data output	DVP_DATA[11]	DVP data lane

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Table 4-1 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO15	SYS_GPIO15	GPIO15	LCD_-DATAOUT[11]	LCD data output	DVP_CLK	DVP clock
GPIO16	SYS_GPIO16	GPIO16	LCD_-DATAOUT[12]	LCD data output	DVP_VSYNC	DVP vertical synchronization
GPIO17	SYS_GPIO17	GPIO17	LCD_-DATAOUT[13]	LCD data output	DVP_HSYNC	DVP horizontal synchronization
GPIO18	SYS_GPIO18	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[14]	LCD data output	DVP_DATA[0]	DVP data lane
GPIO19	SYS_GPIO19	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[15]	LCD data output	DVP_DATA[1]	DVP data lane
GPIO20	SYS_GPIO20	GPIO20	LCD_-DATAOUT[16]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO21	SYS_GPIO21	GPIO21	LCD_-DATAOUT[17]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO22	SYS_GPIO22	GPIO22	LCD_-DATAOUT[18]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO23	SYS_GPIO23	GPIO23	LCD_-DATAOUT[19]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO24	SYS_GPIO24	GPIO24	LCD_-DATAOUT[20]	LCD data output	DVP_DATA[6]	DVP data lane
GPIO25	SYS_GPIO25	GPIO25	LCD_-DATAOUT[21]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO26	SYS_GPIO26	GPIO26	LCD_-DATAOUT[22]	LCD data output	DVP_DATA[8]	DVP data lane
GPIO27	SYS_GPIO27	GPIO27	LCD_-DATAOUT[23]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO28	SYS_GPIO28	GPIO28	NONE	Not defined	DVP_DATA[10]	DVP data lane
GPIO29	SYS_GPIO29	GPIO29	LCD_CLK	LCD clock	DVP_DATA[11]	DVP data lane
GPIO30	SYS_GPIO30	GPIO30	LCD_VSYNC	LCD vertical synchronization	DVP_CLK	DVP clock

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Table 4-1 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO31	SYS_GPIO31	GPIO31	LCD_HSYNC	LCD horizontal synchronization	DVP_VSYNC	DVP vertical synchronization
GPIO32	SYS_GPIO32	GPIO32	LCD_DE	LCD *Data Enable (DE)* mode	DVP_HSYNC	DVP horizontal synchronization
GPIO33	SYS_GPIO33	GPIO33	LCD_-DATAOUT[0]	LCD data output	DVP_DATA[0]	DVP data lane
GPIO34	SYS_GPIO34	GPIO34	LCD_-DATAOUT[1]	LCD data output	DVP_DATA[1]	DVP data lane
GPIO35	SYS_GPIO35	The reset output line of WDT	LCD_-DATAOUT[2]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO36	SYS_GPIO36	The SCL signal trace of I2C	LCD_-DATAOUT[3]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO37	SYS_GPIO37	The SDA signal trace of I2C	LCD_-DATAOUT[4]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO38	SYS_GPIO38	The SCL signal trace of I2C	LCD_-DATAOUT[5]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO39	SYS_GPIO39	The SDA signal trace of I2C	LCD_-DATAOUT[6]	LCD data output	DVP_DATA[6]	DVP data lane
GPIO40	SYS_GPIO40	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[7]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO41	SYS_GPIO41	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[8]	LCD data output	DVP_DATA[8]	DVP data lane
GPIO42	SYS_GPIO42	The modem control *Request To Send (RTS)* output line of UART, Negative	LCD_-DATAOUT[9]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO43	SYS_GPIO43	The *Clear To Send (CTS)* modem status of UART, Negative	LCD_-DATAOUT[10]	LCD data output	DVP_DATA[10]	DVP data lane
GPIO44	SYS_GPIO44	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[11]	LCD data output	DVP_DATA[11]	DVP data lane
GPIO45	SYS_GPIO45	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[12]	LCD data output		

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Table 4-1 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO46	SYS_GPIO46	The modem control *Request To Send (RTS)* output line of UART, Negative	LCD_-DATAOUT[13]	LCD data output		
GPIO47	SYS_GPIO47	The *Clear To Send (CTS)* modem status of UART, Negative	LCD_-DATAOUT[14]	LCD data output		
GPIO48	SYS_GPIO48	The chip select line of SPI, Negative	LCD_-DATAOUT[15]	LCD data output		
GPIO49	SYS_GPIO49	The series clock line of SPI	LCD_-DATAOUT[16]	LCD data output		
GPIO50	SYS_GPIO50	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[17]	LCD data output		
GPIO51	SYS_GPIO51	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[18]	LCD data output		
GPIO52	SYS_GPIO52	The chip select line of SPI, Negative	LCD_-DATAOUT[19]	LCD data output		
GPIO53	SYS_GPIO53	The series clock line of SPI	LCD_-DATAOUT[20]	LCD data output		
GPIO54	SYS_GPIO54	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[21]	LCD data output		
GPIO55	SYS_GPIO55	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[22]	LCD data output		
GPIO56	SYS_GPIO56	The chip select line of SPI, Negative	LCD_-DATAOUT[23]	LCD data output		
GPIO57	SYS_GPIO57	The series clock line of SPI				
GPIO58	SYS_GPIO58	The *Receive Data (RXD)* line of SPI				
GPIO59	SYS_GPIO59	The *Transmit Data (TXD)* line of SPI				
GPIO60	SYS_GPIO60	The chip select line of SPI, Negative				

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Table 4-1 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO61	SYS_GPIO61	The series clock line of SPI				
GPIO62	SYS_GPIO62	The *Receive Data (RXD)* line of SPI				
GPIO63	SYS_GPIO63	The *Transmit Data (TXD)* line of SPI				

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4.2. Full Multiplexing

JH7110 provides full address multiplexing so that SYS_GPIO from SYS_GPIO0 - SYS_GPIO63 in Function 0 can be configured to any of the following signals:

Table 4-2 Full Multiplexing

Signal	Description	Direction	Type	Connect
hifi4_jtag_tck	The TAP clock signal for JTAG on HIFI4	Input	GPIO/Clock	sys_iomux
hifi4_jtag_tdi	The TAP data input signal for JTAG on HIFI4	Input	GPIO	sys_iomux
hifi4_jtag_tdo	The TAP data output signal for JTAG on HIFI4	Output	GPIO	sys_iomux
hifi4_jtag_tms	The TAP mode switch signal for JTAG on HIFI4	Input	GPIO	sys_iomux
hifi4_jtag_trstn	The TAP reset negative signal for JTAG on HIFI4	Input	GPIO	sys_iomux
cdns_qspi_qspi_csn1	The chip select negative signal for QSPI	Output	GPIO	sys_iomux
uart0_rxd	The data receiving signal for UART0	Input	GPIO	sys_iomux
uart0_txd	The data transmission signal for UART0	Output	GPIO	sys_iomux
uart1_cts_n	The *Clear to Send (CTS)* negative signal for UART1	Input	GPIO	sys_iomux
uart1_rts_n	The *Require to Send (RTS)* negative signal for UART1	Output	GPIO	sys_iomux
uart1_rxd	The data receiving signal for UART1	Input	GPIO	sys_iomux
uart1_txd	The data transmission signal for UART1	Output	GPIO	sys_iomux
uart2_cts_n	The *Clear to Send (CTS)* negative signal for UART2	Input	GPIO	sys_iomux
uart2_rts_n	The *Require to Send (RTS)* negative signal for UART2	Output	GPIO	sys_iomux
uart2_rxd	The data transmission signal for UART2	Input	GPIO	sys_iomux
uart2_txd	The data transmission signal for UART2	Output	GPIO	sys_iomux
i2c0_i2c_scl	The clock signal for I2C0	Input/Output	GPIO	sys_iomux
i2c0_i2c_sda	The data transmission signal for I2C0	Input/Output	GPIO	sys_iomux
i2c1_i2c_scl	The clock signal for I2C1	Input/Output	GPIO	sys_iomux
i2c1_i2c_sda	The data transmission signal for I2C1	Input/Output	GPIO	sys_iomux
i2c2_i2c_scl	The clock signal for I2C2	Input/Output	GPIO	sys_iomux
i2c2_i2c_sda	The data transmission signal for I2C2	Input/Output	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
tdm_rx	The receiving signal for TDM	Input	GPIO	sys_iomux
tdm_sync	The synchronization signal for TDM	Input/Output	GPIO	sys_iomux
tdm_tx	The transmission signal for TDM	Output	GPIO	sys_iomux
pdm_4mic_dmic0_din	The data input signal for PDM DMIC0	Input	GPIO	sys_iomux
pdm_4mic_dmic1_din	The data input signal for PDM DMIC1	Input	GPIO	sys_iomux
pdm_4mic_dmic_clk	The clock signal for PDM DMIC	Output	GPIO	sys_iomux
uart3_rxd	The data receiving signal for UART3	Input	GPIO	sys_iomux
uart3_txd	The data transmission signal for UART3	Output	GPIO	sys_iomux
uart4_cts_n	The *Clear to Send (CTS)* negative signal for UART4	Input	GPIO	sys_iomux
uart4_rts_n	The *Require to Send (RTS)* negative signal for UART4	Output	GPIO	sys_iomux
uart4_rxd	The data receiving signal for UART3	Input	GPIO	sys_iomux
uart4_txd	The data transmission signal for UART4	Output	GPIO	sys_iomux
uart5_cts_n	The *Clear to Send (CTS)* negative signal for UART5	Input	GPIO	sys_iomux
uart5_rts_n	The *Require to Send (RTS)* negative signal for UART5	Output	GPIO	sys_iomux
uart5_rxd	The data receiving signal for UART5	Input	GPIO	sys_iomux
uart5_txd	The data transmission signal for UART5	Output	GPIO	sys_iomux
i2c3_scl	The clock signal for I2C3	Input/Output	GPIO	sys_iomux
i2c3_sda	The data transmission signal for I2C3	Input/Output	GPIO	sys_iomux
i2c4_scl	The clock signal for I2C4	Input/Output	GPIO	sys_iomux
i2c4_sda	The data transmission signal for I2C4	Input/Output	GPIO	sys_iomux
i2c5_scl	The clock signal for I2C5	Input/Output	GPIO	sys_iomux
i2c5_sda	The data transmission signal for I2C5	Input/Output	GPIO	sys_iomux
i2c6_scl	The clock signal for I2C6	Input/Output	GPIO	sys_iomux
i2c6_sda	The data transmission signal for I2C6	Input/Output	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
spi0_ssp_sclk	The clock signal for SPI0	Input/Output	GPIO	sys_iomux
spi0_ssp_csn	The chip select negative signal for SPI0	Input/Output	GPIO	sys_iomux
spi0_ssp_rxd	The data receiving signal for SPI0	Input	GPIO	sys_iomux
spi0_ssp_txd	The data transmission signal for SPI0	Output	GPIO	sys_iomux
spi1_ssp_sclk	The clock signal for SPI1	Input/Output	GPIO	sys_iomux
spi1_ssp_csn	The chip select negative signal for SPI1	Input/Output	GPIO	sys_iomux
spi1_ssp_rxd	The data receiving signal for SPI1	Input	GPIO	sys_iomux
spi1_ssp_txd	The data transmission signal for SPI1	Output	GPIO	sys_iomux
spi2_ssp_sclk	The clock signal for SPI2	Input/Output	GPIO	sys_iomux
spi2_ssp_csn	The chip select negative signal for SPI2	Input/Output	GPIO	sys_iomux
spi2_ssp_rxd	The data receiving signal for SPI2	Input	GPIO	sys_iomux
spi2_ssp_txd	The data transmission signal for SPI2	Output	GPIO	sys_iomux
spi3_ssp_sclk	The clock signal for SPI3	Input/Output	GPIO	sys_iomux
spi3_ssp_csn	The chip select negative signal for SPI3	Input/Output	GPIO	sys_iomux
spi3_ssp_rxd	The data receiving signal for SPI3	Input	GPIO	sys_iomux
spi3_ssp_txd	The data transmission signal for SPI3	Output	GPIO	sys_iomux
spi4_ssp_sclk	The clock signal for SPI4	Input/Output	GPIO	sys_iomux
spi4_ssp_csn	The chip select negative signal for SPI4	Input/Output	GPIO	sys_iomux
spi4_ssp_rxd	The data receiving signal for SPI4	Input	GPIO	sys_iomux
spi4_ssp_txd	The data transmission signal for SPI4	Output	GPIO	sys_iomux
spi5_ssp_sclk	The clock signal for SPI5	Input/Output	GPIO	sys_iomux
spi5_ssp_csn	The chip select negative signal for SPI5	Input/Output	GPIO	sys_iomux
spi5_ssp_rxd	The data receiving signal for SPI5	Input	GPIO	sys_iomux
spi5_ssp_txd	The data transmission signal for SPI5	Output	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
spi6_ssp_sclk	The clock signal for SPI6	Input/Output	GPIO	sys_iomux
spi6_ssp_csn	The chip select negative signal for SPI6	Input/Output	GPIO	sys_iomux
spi6_ssp_rxd	The data receiving signal for SPI6	Input	GPIO	sys_iomux
spi6_ssp_txd	The data transmission signal for SPI6	Output	GPIO	sys_iomux
pwm[0]	The PWM 0 signal	Output	GPIO	sys_iomux
pwm[1]	The PWM 1 signal	Output	GPIO	sys_iomux
pwm[2]	The PWM 2 signal	Output	GPIO	sys_iomux
pwm[3]	The PWM 3 signal	Output	GPIO	sys_iomux
pwm[4]	The PWM 4 signal	Output	GPIO	aon_iomux
pwm[5]	The PWM 5 signal	Output	GPIO	aon_iomux
pwm[6]	The PWM 6 signal	Output	GPIO	aon_iomux
pwm[7]	The PWM 7 signal	Output	GPIO	aon_iomux
sys_crg_clk_jtag_tck	The TAP clock signal for JTAG on System CRG clock	Input	GPIO	sys_iomux
clkrst_src_bypass_jtag_trstn	The TAP reset negative signal for JTAG on clock reset source bypass	Input	GPIO	sys_iomux
jtag_certification_tdi	The TAP data input signal for JTAG on Certification	Input	GPIO	sys_iomux
jtag_certification_tdo	The TAP data output signal for JTAG on Certification	Output	GPIO	sys_iomux
jtag_certification_tms	The TAP mode switch signal for JTAC on Certification	Input	GPIO	sys_iomux
sdio0_back_end_power	The back end power signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_int_n	The card initialization negative signal for SDIO0	Input	GPIO	sys_iomux
sdio0_card_power_en	The card power supply signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_write_prt	The card data write signal for SDIO0	Input	GPIO	sys_iomux
sdio0_card_rst_n	The card reset negative signal for SDIO0	Output	GPIO	sys_iomux
sdio0_ccmd_od_pullup_en_n	The pullup enable signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_detect_n	The card detect negative signal for SDIO0	Input	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
sdio1_back_end_power	The back end power signal for SDIO1	Output	GPIO	sys_iomux
sdio1_card_int_n	The card initialization negative signal for SDIO1	Input	GPIO	sys_iomux
sdio1_card_power_en	The card power supply signal for SDIO1	Output	GPIO	sys_iomux
sdio1_card_write_prt	The card data write signal for SDIO1	Input	GPIO	sys_iomux
sdio1_clk	The clock signal for SDIO1	Output	GPIO	sys_iomux
sdio1_ccmd	The Command signal of SDIO1	Input/Output	GPIO	sys_iomux
sdio1_cdata[0]	The Data 0 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[1]	The Data 1 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[2]	The Data 2 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[3]	The Data 3 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[4]	The Data 4 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[5]	The Data 5 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[6]	The Data 6 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[7]	The Data 7 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_card_rst_n	The card reset signal of SDIO1	Output	GPIO	sys_iomux
sdio1_ccmd_od_pullup_en_n	The pullup enable signal for SDIO1	Output	GPIO	sys_iomux
sdio1_data_strobe	The data strobe signal for SDIO1	Input	GPIO	sys_iomux
sdio1_card_detect_n	The card detect signal for SDIO1	Input	GPIO	sys_iomux
sys_crg_ext_mclk	The external main clock signal for System CRG.	Input	GPIO	sys_iomux
sys_crg_mclk_out	The main clock output signal for System CRG.	Output	GPIO	sys_iomux
sys_crg_clk_gmac_phy	The GMAC PHY signal for System CRG.	Output	GPIO	sys_iomux
sys_crg_i2stx_bclk_mst	The bit clock master signal for I2S Transmission	Output	GPIO	sys_iomux
sys_crg_i2stx_lrck_mst	The left-right clock (frame clock) master signal for I2S Transmission	Output	GPIO	sys_iomux
sys_crg_i2srx_bclk_mst	The bit clock master signal for I2S Receiving	Output	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
sys_crg_i2srx_lrck_mst	The left-right clock (frame clock) master signal for I2S Receiving	Output	GPIO	sys_iomux
sys_crg_i2stx_bclk_slv	The bit clock slave signal for I2S Transmission	Input	GPIO	sys_iomux
sys_crg_i2stx_lrck_slv	The left-right clock (frame clock) slave signal for I2S Transmission	Input	GPIO	sys_iomux
sys_crg_i2srx_bclk_slv	The bit clock slave signal for I2S Receiving	Input	GPIO	sys_iomux
sys_crg_i2srx_lrck_slv	The left-right clock (frame clock) slave signal for I2S Receiving	Input	GPIO	sys_iomux
sys_crg_tdm_clk_slv	The TDM slave clock signal for System CRG	Input	GPIO	sys_iomux
sys_crg_tdm_clk_mst	The TDM master clock signal for System CRG	Output	GPIO	sys_iomux
aon_crg_clk_32k_out	The clock 32K output signal for AON CRG	Output	GPIO	aon_iomux
i2stx_4ch_sdo0	The Sound Output 0 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo1	The Sound Output 1 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo2	The Sound Output 2 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo3	The Sound Output 3 for I2S	Output	GPIO	sys_iomux
audio_i2srx_ext_sdin0	The Sound Input 0 for I2S	Input	GPIO	sys_iomux
audio_i2srx_ext_sdin1	The Sound Input 1 for I2S	Input	GPIO	sys_iomux
audio_i2srx_ext_sdin2	The Sound Input 2 for I2S	Input	GPIO	sys_iomux
sys_crg_clk_gclk0	The Global Clock 0 signal for System CRG	Output	GPIO	aon_iomux
sys_crg_clk_gclk1	The Global Clock 1 signal for System CRG	Output	GPIO	aon_iomux
sys_crg_clk_gclk2	The Global Clock 2 signal for System CRG	Output	GPIO	aon_iomux
spdif_spdifi	The input signal for SPDIF	Input	GPIO	sys_iomux
spdif_spdifo	The output signal for SPDIF	Output	GPIO	sys_iomux
vout_hdmi_tx_cec_sda	The serial data CEC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_ddc_scl	The serial clock DDC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_ddc_sda	The serial data DDC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_hdmitx_hpd	The *Hot Plug Detect (HPD)* signal for HDMI Transmission	Input	GPIO	sys_iomux

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Table 4-2 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
usb_drive_vbus_io	The VBUS (power supply + cable) input/output signal for USB	Output	GPIO	sys_iomux
usb_overcurrent_n_io	The over-current input/output signal for USB	Input	GPIO	sys_iomux
u7mc_sft7110_tref	The Timer Reference signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[0]	The Timer Data 0 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[1]	The Timer Data 1 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[2]	The Timer Data 2 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[3]	The Timer Data 3 signal for U74 MC	Output	GPIO	sys_iomux
WAVE511_i_uart_rxsin	The UART receiving input signal for WAVE511	Input	GPIO	sys_iomux
WAVE511_o_uart_txsout	The UART transmission input signal for WAVE511	Output	GPIO	sys_iomux
GPIO_wakeup[3]	The GPIO Wakeup 3 signal	Input	GPIO	aon_iomux
GPIO_wakeup[2]	The GPIO Wakeup 2 signal	Input	GPIO	aon_iomux
GPIO_wakeup[1]	The GPIO Wakeup 1 signal	Input	GPIO	aon_iomux
GPIO_wakeup[0]	The GPIO Wakeup 0 signal	Input	GPIO	aon_iomux
can_ctrl0_can_txd	The data transmission signal for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl0_can_rxd	The data receiving signal for CAN Controller 0	Input	GPIO	sys_iomux
can_ctrl1_can_stby	The standby signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_can_txd	The data transmission signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_can_rxd	The data receiving signal for CAN Controller 1	Input	GPIO	sys_iomux
can_ctrl1_can_stby	The standby signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl0_tst_sample_point	The test sample point for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl0_tst_next_bit	The test next point for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl1_tst_sample_point	The test sample point for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_tst_next_bit	The test next point for CAN Controller 1	Output	GPIO	sys_iomux
dskit_wdt_rstout	The reset output signal for WDT	Output	GPIO	sys_iomux

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5. Power and Clocking

5.1. Power Supply

5.1.1. Power-Up Sequence

JH7110 has 3 power supplies, VDD, AVDL, and AVDH. VDD and AVDL are both core power supplies and while separate pins are used for noise isolation purposes.

The recommended power sequence is that from digital core voltage to analog I/O voltage and from low voltage level to high voltage level. This is not considered a constraint, but instead, a guideline, as it could result in the best-case operating scenario, where the leakage currents during power up are kept to a minimum.

The following diagram shows the recommended power-on sequence of different power groups.

Figure 5-1 Power Up Sequence

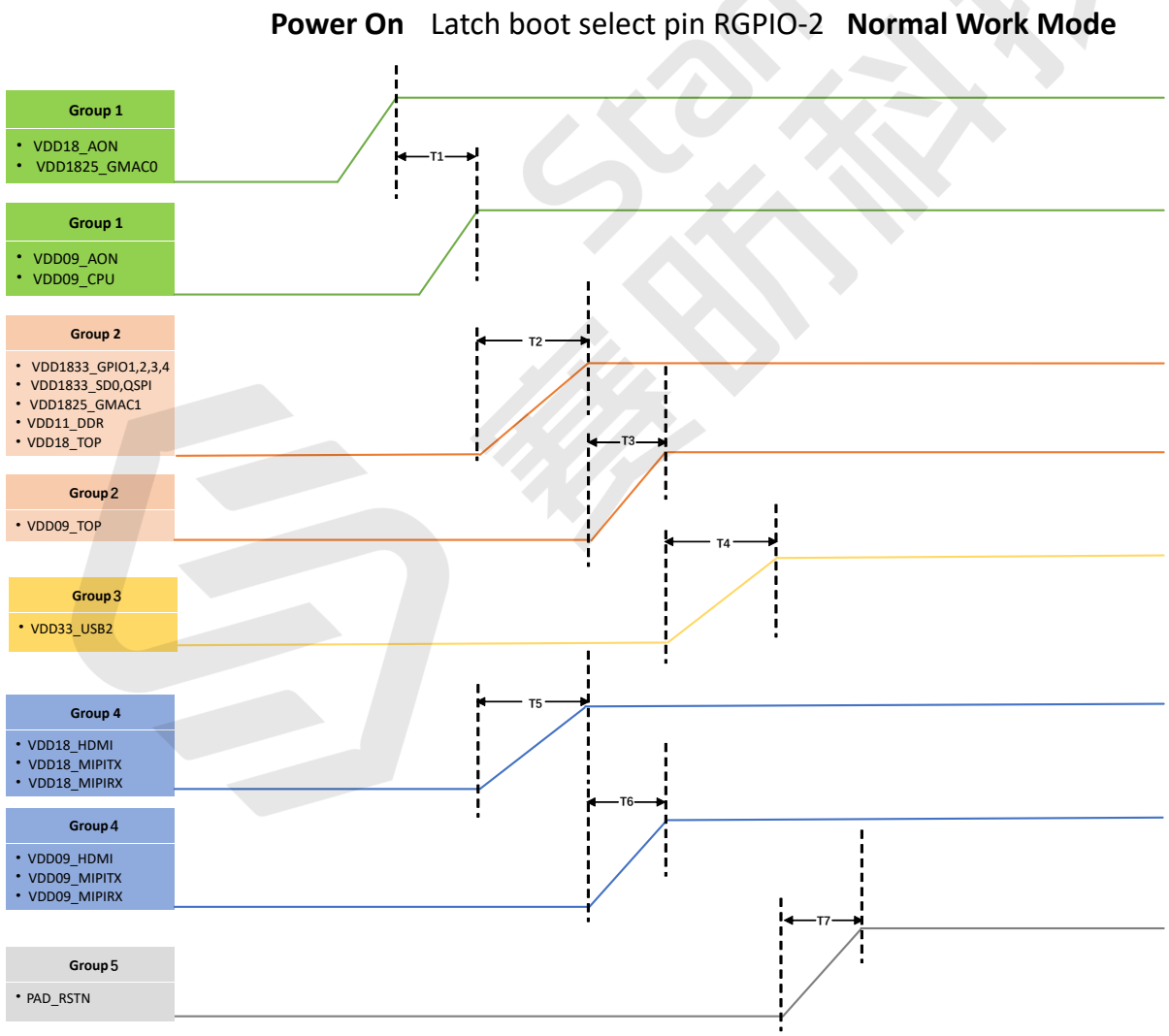

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Table 5-1 Power Up Sequence Intervals

Sequence	Interval
T1	100 us
T2	300-500 us
T3	50-100 us
T4	300-500 us
T5	300-500 us
T6	50-100 us
T7	>10 ms

5.1.2. Power Pin Voltage

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The following table shows the voltage information for each power pin.

Table 5-2 Power Pin Voltage Information

Power Pin in PMIC	Package Ball Name	Power Pin Index	Voltage (V)	Comment
VDD09_AON	VDD	1	0.9	Standby mode, all AON relevant power supplies should be on and all others off.
	VDD_RTC			
VDD09_CPU	VDD_CPU	2	0.9 to 1.0	CPU core power supply, which can be adjusted to 1.0 V
VDD18_AON	VDD18_OSC	3	1.8	AON domain GPIO, RPIO,RESETN,TESTEN,1.8 V only
	VDD18_OTP			
	VDD1833_AON			
VDD1825_GMAC0	VDD1825_GMAC0	4	1.8/2.5	IO voltage for GMAC0, 1.8 V and 2.5 V switchable, AON domain
VDD18_HDMI	AVDD_HDMI	5	1.8	HDMI and MIPITX 1.8 V analog power supply which should be powered on first
VDD09_HDMI	AVDD09_HDMI	6	0.9	The 0.9 V voltage for Core, PLL, MIPI, and so on, should be powered on after VDD18_HDMI_MIPITX. VDD09_HDMI should be powered on together with VOUT digital.
	PVDD_HDMI			
VDD18_MIPITX	VCC18A_MIPITX	7	1.8	
VDD09_MIPITX	VDD_MIPITX	8	0.9	
VDD18_MIPIRX	VCC18A_MIPIRX	9	1.8	MIPI RX 1.8 V analog power supply which should be powered on first
VDD09_MIPIRX	VCC09A_MIPIRX	10	0.9	MIPI RX 0.9 V power supply, which should be powered on after VDD18_MIPIRX
VDD33_USB2	VCCA33_USB	11	3.3	3.3 V USB interface voltage, which should be powered on after the 1.8 V and 0.9 V voltage, and powered off first.
VDD09_TOP	AVDD09_USB	12	0.9	
	AVDL_PCIE0			
	AVDL_PCIE1			
	VDD_PLL0			
	VDD_PLL1			
	VDD_PLL2			

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Table 5-2 Power Pin Voltage Information (continued)

Power Pin in PMIC	Package Ball Name	Power Pin Index	Voltage (V)	Comment
	VDD_DDR			DDR PHY core power 0.9 V
	VDDPLL_DDR			DDR PHY PLL power 0.9 V
VDD18_TOP	VCCA18_PLL0	13	1.8	
	VCCA18_PLL1			
	VDD18_TEMP			
	VDDA18_TEMP			
	VCCA18_PLL2			
	AVDH_PCIE0			
	AVDH_PCIE1			
	VCCA18_USB			
VDDQ11_DDR	VDDQ_DDR	14	1.1	DDR PHY IO and clock IO voltage, 1.1 V
	VDDQCK_DDR			
VDD1833_GPIO1	VDD1833_GPIO1	15	1.8/3.3	GPIO Group 1 voltage, 1.8 V and 3.3 V switchable
VDD1833_GPIO2	VDD1833_GPIO2			GPIO Group 2 voltage, 1.8 V and 3.3 V switchable
VDD1833_GPIO3	VDD1833_GPIO3			GPIO Group 3 voltage, 1.8 V and 3.3 V switchable
VDD1833_GPIO4	VDD1833_GPIO4	16		GPIO Group 4 voltage, 1.8 V and 3.3 V switchable
VDD1833_SD0	VDD1833_SD0			SD0 IO voltage, 1.8 V and 3.3 V switchable
VDD1833_QSPI	VDD1833_QSPI	16	1.8/3.3	QSPI IO voltage, 1.8 V and 3.3 V switchable
VDD1825_GMAC1	VDD1825_GMAC1	17	1.8/2.5	GMAC IO voltage, 1.8 V and 2.5 V switchable

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Make sure you understand the following statements.

1. Every power pin stands for a PMIC/DC-DC power output, whose ON/OFF, sequence, voltage, etc. have to be controlled separately. Since GPIO, SD, and QSPI may have up to 2 power voltages, there can be in total 17 power outputs.
2. CPU uses I2C (GPIO) to configure all PMIC relevant parameters.

For Hot Reset: Follow the same procedure as the cold powering-up, but only remember not to switch off the AON power supplies.

5.1.3. Power Group Description

Table 5-3 Power Group Description

Group	Name	Dir	Description
Analog P/G	AVDH	PAD	1.8 V analog power supply
	AVDL	PAD	0.9 V analog power supply
	AVSS	PAD	Analog ground
High-Speed Signal	RXP	PAD	Differential data input of RX, positive
	RXN	PAD	Differential data input of RX, negative
	TXP	PAD	Differential data output of TX, positive
	TXN	PAD	Differential data output of TX, negative
Reference Clock Input/Output	CKREFP	PAD	Differential pair that can be configured as either a reference clock input or a reference clock output, P for positive and N for negative.
	CKREFN	PAD	
Digital P/G	VDD/VDDA/VDDB	PIN	VDD/VSS – Digital Power from the core inside. VDDA/VDDB/VSSA/VSSB – PIN of Power Cut IO between Analog Power Domain and Digital Power Domain.
	VSS/VSSA/VSSB	PIN	

5.2. Clock and Reset

5.2.1. Reset Source

System includes the following reset sources.

Table 5-4 Reset Source

Source	Description
Pad	Used to reset the whole chip.
Watchdog	Used to reset the whole chip and all outputs to PAD.
Software reset in system top	Used to reset all logic modules except the “always-on” domain.
Software reset in the “always-on” domain	Used to reset the whole chip.
Low power **rstn**	Used to reset each power domain separately.

5.2.2. Reset Sequence

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Follow the sequence below to reset the JH7110 system.

Table 5-5 Reset Sequence

Sequence	Description
1	Powering up the chip, resetting the pad to active, and then latching the boot selection signals. The reset sequence starts after pad is reset to high.
2	5us delay, release the always-on domain reset, and clocks generated in always-on domain. And release the reset source on **dom_sys_top**.
3	Power down the PLL with 2us time interval
4	After the PLL power-down has been finished, wait 200us for PLL locking.
5	64 cycles of oscillator clock delay, release the system *Clock and Reset Generator (CRG)*'s reset to prepare the clock for system
6	64 cycles of oscillator clock delay, and release the system bus reset
7	Release CPU core reset after 32 cycles of oscillator clock delay has been completed. And CPU will boot from the boot vector.

5.2.3. Clock Structure

The clock and reset structure of JH7110 is displayed in the following diagram.

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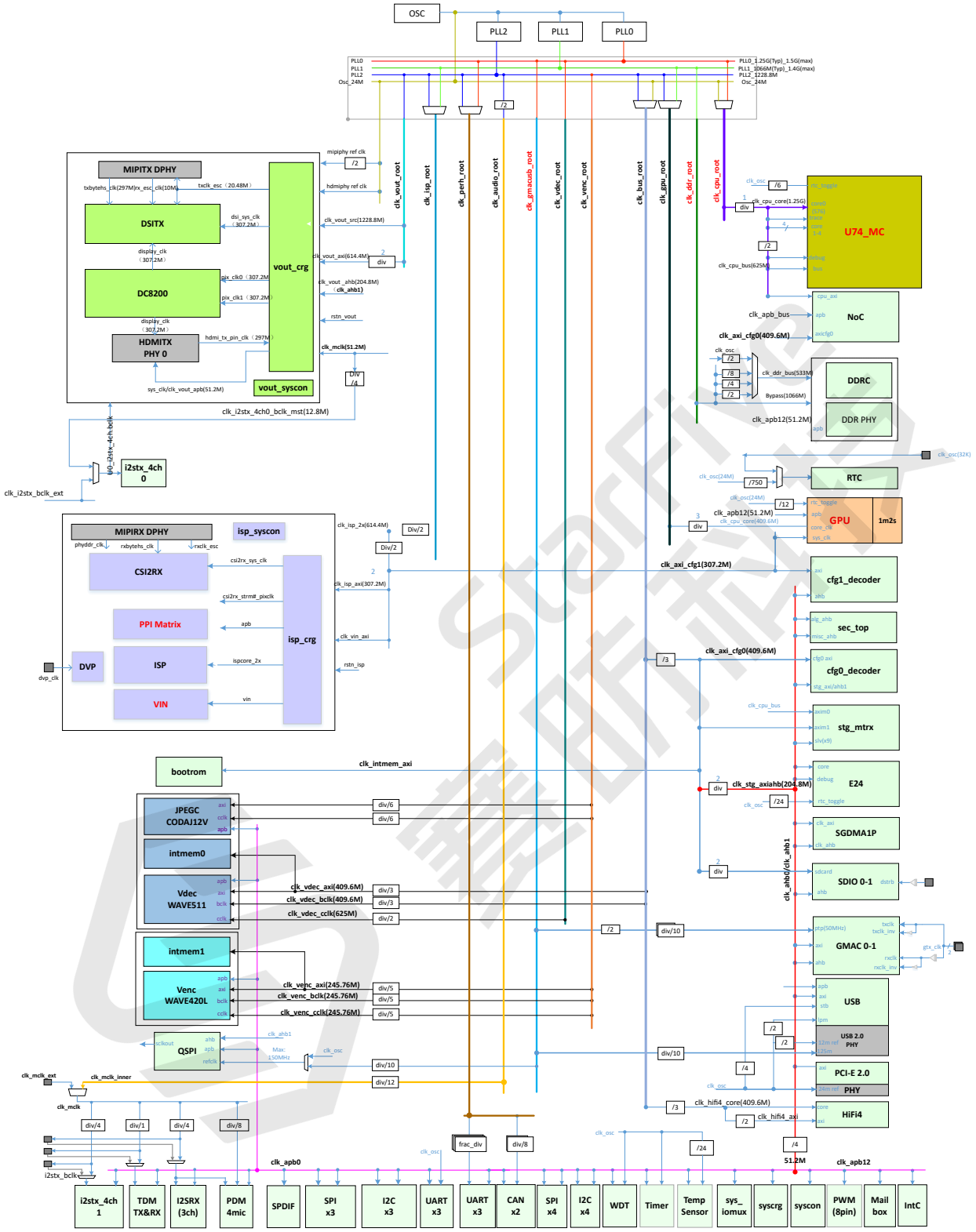
Figure 5-2 Clock Structure



5.2.4. System PLL

JH7110 system includes 3 PLLs, and the REFCLK is 24 MHz from external crystal.

The PLL clock frequency block diagram is shown in the following diagram.

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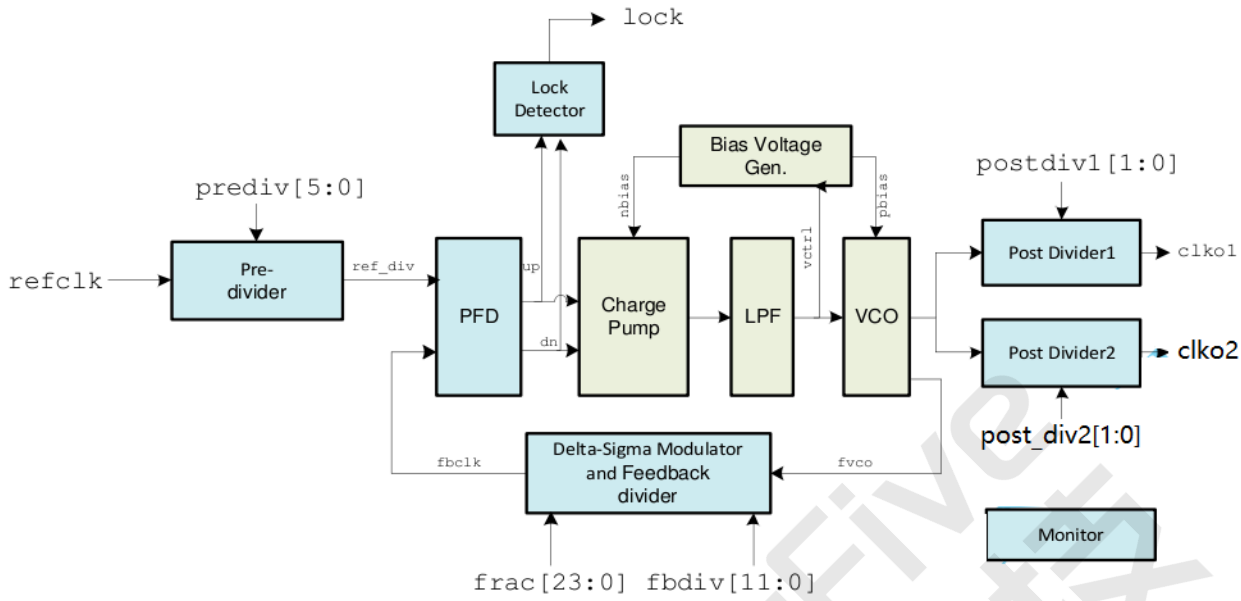
Figure 5-3 System PLL



PLL supports integer and fraction multiple, you should set **dacpd** and **dsmpd** to high while integer multiple mode, and set both them to low while fraction multiple mode.

Inter Multiple Mode

Both **dacpd** and **dsmpd** should be set as 1 while integer multiple mode.

The frequency of outputs can be figured out as below.

Fvco = Fref × NI ÷ M

NI is integer frequency dividing ratio of feedback divider, set by fbdiv[1:0] , NI = 8, 9, 10, 12, 13, …, 4095

M is frequency dividing ratio of pre-divider, set by prediv[5:0], M = 1, 2, …, 63

Fclkol = Fvco ÷ Ql

Q1 is frequency dividing ratio of post divider, set by postdiv[l:0], Ql = 1, 2, 4, 8

Fclko2 = Fvco ÷ Q2

Q2 is frequency dividing ratio of post divider, set by postdiv2[l:0], Q2= 1, 2, 4, 8

Fraction Multiple Mode

Both **dacpd** and **dsmpd** should be set as 0 while integer multiple mode.

Fvco = Fref × (NI+NF)÷M

NI is integer frequency dividing ratio of feedback divider, set by fbdivf 11:0] , NI = 8, 9, 10, 12, 13, …, 4095

NF is fractional frequency dividing ratio, set by frac[0:23]. NF =frac[0:23]/2^24 = 0 - 0.99999994

M is frequency dividing ratio of pre-divider, set by prediv[5:0], M = 1, 2, …, 63

Fclkol = Fvco ÷ Ql

Ql is frequency dividing ratio of post divider, set by postdivl [1:0],Q1 = 1, 2, 4, 8

Fclko2 = Fvco ÷ Q2

Q2 is frequency dividing ratio of post divider, set by postdiv2[1:0],Q2= 1, 2, 4, 8

5.2.5. Clock Specification

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The clock specification of JH7110 is displayed in the following table.

Table 5-6 Clock Specifications

Module	Max (MHz)	Comment
U74	1,500	
GPU	400	
DDR	1,400	
JPEG Codec	200	
Video Decoder	400	
Video Encoder	250	
SGDMA	200	
AHB	200	
APB	50	
Display AXI	600	
MIPI and HDMI Pixel Clock	297	4K-30fps
LCD	74.25	1080p-30fps
ISP	300	
PCI-E	200	
USB	200	

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6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage the device.

Symbol	Parameters	Min	Max	Units
VDD	Power supply for Core	0.81	0.99	V
VDDIO	Power supply for Post-Driver	-0.5	3.63	V
Tj	Junction temperature	0	125	℃
Ts	Storage temperature	-40	125	℃

6.2. Recommended Operating Conditions

Table 6-2 Recommended DC Operating Conditions

Power Pin	Ground	Description	Min	Typ	Max	Unit
VDD	VSS	Core power supply	0.81	0.9	0.99	V
VDD18		Digital IO power supply	1.62	1.8	1.98	V
VDD33		Digital function IO power supply	3.135	3.3	3.465	V
AVDD18_MIPITX	VSS	MIPI TX analog power supply	1.62	1.8	1.98	V
AVDD18_MIPIRX	AVSS_MIPIRX	MIPI RX analog power supply for LDO	1.62	1.8	1.98	V
AVDD09_MIPIRX		MIPI RX analog power supply	0.855	0.9	0.99	V
AVDD18_TS	VSS18_TS	Temperature sensor analog power supply	1.62	1.8	1.98	V
AVDD33_USB	AVSS_USB	USB analog power supply	2.97	3.3	3.63	V
AVDD18_USB		USB analog power supply	1.62	1.8	1.98	V
AVDD18_PCIE	AVSS_PCIE	USB TX analog power supply	1.62	1.8	1.98	V

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Table 6-2 Recommended DC Operating Conditions (continued)

Power Pin		Ground	Description	Min	Typ	Max	Unit
AVDD09TX_PCIE		AVSS09TX_PCIE	PCIE TX analog power supply	0.85	0.9	0.95	V
AVDD09RX_PCIE		AVSS09RX_PCIE	PCIE RX analog power supply	0.85	0.9	0.95	V
AVDD18_HDMI		AVSS18_HDMI	HDMI analog power supply	1.62	1.8	1.98	V
AVDD09P_HDMI		AVSS09P_HDMI	HDMI analog power supply of PLL	0.81	0.9	0.99	V
AVDD09D_HDMI		AVSS09D_HDMI	HDMI analog power supply of data channel	0.81	0.9	0.99	V
DVDD18_OTP		VSS18_OTP	OTP power supply	1.62	1.8	1.98	V
AVDD09_PLL0		AVSS_PLL0	PLL0 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL1		AVSS_PLL1	PLL1 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL2		AVSS_PLL2	PLL2 analog power supply	0.81	0.9	0.99	V
DDR4/LPDDR4	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDQCK_DDR0		DDR0 CK power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
DDR3/LPDDR3	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDQCK_DDR0		DDR0 CK power supply	1.425/1.14	1.5/1.2	1.575/1.3	V

Note:

1. Power supply voltage beyond operating range is not guaranteed.
2. Power/Ground bouncing beyond DC operating range may cause invalid data output. It is not guaranteed by eMemory and customers must ensure power stability on their own.
3. Normally operating conjunction temperature is from -40 ℃ to 125 ℃ and Program operation should be at conjunction temperature -40 ℃ to 125 ℃.

6.3. Static Power Consumption

The static power consumption of JH7110 is 130 mW.

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6.4. DC Electrical Characteristics

Table 6-3 DC Electrical Characteristics (VDDIO=1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low-Level Voltage	-0.3	-	0.35 × VDDIO	V
VIH	Input High-Level Voltage	0.65 × VDDIO	-	VDDIO + 0.3	V
VT+	Hysteresis Threshold up	0.4 × VDDIO	-	0.7 × VDDIO	V
VT-	Hysteresis Threshold down	0.3 × VDDIO	-	0.6 × VDDIO	V
Vhys	Input Hysteresis Voltage	0.1 × VDDIO	-	0.4 × VDDIO	V
Rpu	Pull-up Resistor				Ω
Rpd	Pull-down Resistor				Ω
VOL	Output Low-Level Voltage	-	-	0.45	V
VOH	Output High-Level Voltage	1.35	-	-	V
IOL	Low Level Output Current @VOL (Max)				
	Drive Strength (E2, E1=00)	3.3	4.9	8.8	mA
	Drive Strength (E2, E1=01)	7.7	11.5	20.5	mA
	Drive Strength (E2, E1=10)	13.2	19.7	35.0	mA
	Drive Strength (E2, E1=11)	17.6	26.2	46.7	mA
IOH	High-Level Output Current @VOH (Min)				
	Drive Strength (E2, E1=00)	3.6	5	7.7	mA
	Drive Strength (E2, E1=01)	7.1	10	15.4	mA
	Drive Strength (E2, E1=10)	13.1	18.3	28.3	mA
	Drive Strength (E2, E1=11)	16.6	23.2	36.0	mA

Table 6-4 DC Electrical Characteristics (VDDIO=2.5V)

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Level Voltage	-0.3	-	0.7	V

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Table 6-4 DC Electrical Characteristics (VDDIO=2.5V) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
VIH	Input High Level Voltage	1.7	-	VDDIO + 0.3	V
VT+	Hysteresis Threshold up	0.9	-	1.7	V
VT-	Hysteresis Threshold down	0.7	-	1.5	V
Vhys	Input Hysteresis Voltage	0.2	-	1.0	V
Rpu	Pull-up Resistor				Ω
Rpd	Pull-down Resistor				Ω
VOL	Output Low-Level Voltage	-	-		V
VOH	Output High-Level Voltage		-	-	V
IOL	Low Level Output Current @VOL (Max)				
	Drive Strength (E2, E1=00)	3.7	5.3	9.1	mA
	Drive Strength (E2, E1=01)	8.5	12.3	21.1	mA
	Drive Strength (E2, E1=10)	14.5	21.0	36.2	mA
	Drive Strength (E2, E1=11)	19.3	28.0	48.3	mA
IOH	High-Level Output Current @VOH (Min)				
	Drive Strength (E2, E1=00)	4.1	5.1	7.8	mA
	Drive Strength (E2, E1=01)	8.0	10.2	15.7	mA
	Drive Strength (E2, E1=10)	13.1	18.6	28.7	mA
	Drive Strength (E2, E1=11)	16.7	23.7	36.6	mA

Table 6-5 DC Electrical Characteristics (VDDIO=3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Level Voltage	-0.3	-	0.8	V
VIH	Input High Level Voltage	2	-	VDDIO + 0.3	V
VT+	Hysteresis Threshold up	0.9	-	2.1	V
VT-	Hysteresis Threshold down	0.7	-	1.9	V

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Table 6-5 DC Electrical Characteristics (VDDIO=3.3V) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
Vhys	Input Hysteresis Voltage	0.2	-	1.4	V
Rpu	Pull-up Resistor				Ω
Rpd	Pull-down Resistor				Ω
VOL	Output Low-Level Voltage	-	-		V
VOH	Output High-Level Voltage		-	-	V
IOL	Low Level Output Current @VOL (Max)				
	Drive Strength (E2, E1=00)	3.4	5.0	8.5	mA
	Drive Strength (E2, E1=01)	8.0	11.6	19.7	mA
	Drive Strength (E2, E1=10)	13.6	19.8	33.8	mA
	Drive Strength (E2, E1=11)	18.1	26.4	45.1	mA
IOH	High-Level Output Current @VOH (Min)				
	Drive Strength (E2, E1=00)	3.3	4.8	7.5	mA
	Drive Strength (E2, E1=01)	6.6	9.5	15.0	mA
	Drive Strength (E2, E1=10)	12.2	17.4	27.5	mA
	Drive Strength (E2, E1=11)	15.5	22.1	34.7	mA

6.5. Maximum Current Consumption

Table 6-6 Maximum Current Consumption

Type	Power	Ground	Attribute	Voltage (V)			Current (mA)			Description
				Min	Typ	Max	Min	Typ	Max	
CORE	VDD	VSS	AON	0.81	0.9	0.99	10	900	1,000	Core power supply for AON modules and the top layer
	VDD_CPU	VSS	AON	0.81	0.9	1		1,000	2,000	CPU power supply, which could be up-scaled to 1.0V
GPIO	VDD1825_GMAC1	VSS		1.62/2.25	1.8/2.5	1.98/2.75	-	4	20	

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Table 6-6 Maximum Current Consumption (continued)

Type	Power	Ground	Attribute	Voltage (V)			Current (mA)			Description
				Min	Typ	Max	Min	Typ	Max	
	VDD1825_GMAC0	VSS	AON	1.62/2.25	1.8/2.5	1.98/2.75	-	4	20	GMAC0 is in AON
	VDD1833_AON	VSS	AON	1.62	1.8	1.98	-	4	20	The AON RGPIO is 1.8V only
	VDD1833_GPIO1	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
	VDD1833_GPIO2	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
	VDD1833_GPIO3	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
	VDD1833_GPIO4	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
SD0/ eMMC	VDD1833_SD0	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
QSPI	VDD1833_QSPI	VSS		1.62/2.97	1.8/3.3	1.98/3.63	-	4	20	
PLL	VDD_PLL0	VSS_PLL0		0.81	0.9	0.99	-	-	5	PLL analog power supply
	VDD_PLL1	VSS_PLL1		0.81	0.9	0.99	-	-	5	PLL analog power supply
	VDD_PLL2	VSS_PLL2		0.81	0.9	0.99	-	-	5	PLL analog power supply
	VCCA18_PLL0	VSS_PLL0		1.62	1.8	1.98	-	-	10	PLL analog power supply
	VCCA18_PLL1	VSS_PLL1		1.62	1.8	1.98	-	-	10	PLL analog power supply
	VCCA18_PLL2	VSS_PLL2		1.62	1.8	1.98	-	-	10	PLL analog power supply
OSC	VDD_RTC	VSS_RTC	AON	0.81	0.9	0.99	-	-	2.5	
	VDD18_OSC	VSS18_OSC	AON	1.62	1.8	1.98	-	4	4	
OTP	VDD18_OTP	VSS18_OTP	AON	1.62	1.8	1.98	-	4	4	
LPDDR4	VDDPLL_DDR	VSS		0.81	0.9	0.99	-	10	100	DDR PLL power supply
	VDDQ_DDR	VSS		1.14/1.06	1.2/1.1	1.26/1.17	-	200	800	VDDQ DDR IO power supply
	VDDQCK_DDR	VSS		1.14/1.06	1.2/1.1	1.26/1.17	-	64	200	DDR CK power supply
	VDD_DDR	VSS		0.81	0.9	0.99	-	10	600	Net name of VDD_DDR is the core power supply for DDR PHY
HDMI	AVDD_HDMI	AVSS_HDMI		1.62	1.8	1.98	-	20	40	

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Table 6-6 Maximum Current Consumption (continued)

Type	Power	Ground	Attribute	Voltage (V)			Current (mA)			Description
				Min	Typ	Max	Min	Typ	Max	
	AVDD09_HDMI	AVSS_HDMI		0.81	0.9	0.99	-	12	40	
	PVDD_HDMI	PVSS_HDMI		0.81	0.9	0.99	-	8	150	
USB	AVDD09_USB	AVSS_USB		0.81	0.9	0.99	-	12	18	
	VCCA18_USB	AVSS_USB		1.62	1.8	1.98	-	9	20	
	VCCA33_USB	AVSS_USB		2.97	3.3	3.63	-	5	20	
Temp Sensor	VDD18_TEMP	VSS18_TEMP		1.62	1.8	1.98	-	2	12	
	VDDA18_TEMP	VSS18_TEMP		1.62	1.8	1.98	-	2	20	
PCIE	AVDH_PCIE0	AVSS_PCIE0		1.62	1.8	1.98	-	20	40	
	AVDL_PCIE0	AVSS_PCIE0		0.81	0.9	0.99	-	12	40	
	AVDH_PCIE1	AVSS_PCIE1		1.62	1.8	1.98	-	20	40	
	AVDL_PCIE1	AVSS_PCIE1		0.81	0.9	0.99	-	12	40	
MIPI RX	VCC09A_MIPIRX	GND09A_MIPIRX		0.855	0.9	0.99	-	4.5	40	
	VCC18A_MIPIRX	GND09A_MIPIRX		1.62	1.8	1.98	-	8	40	
MIPI TX	VDD_MIPITX	VSS		0.855	0.9	0.99	-	4.5	40	
	VCC18A_MIPITX	VSS_MIPITX		1.62	1.8	1.98	-	8	40	

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7. Mechanical Characteristics

7.1. Thermal

7.1.1. Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125 ℃.

7.1.2. Thermal Characteristics

The following table provides the thermal resistance characteristics for the package.

Table 7-1 Thermal Resistance Characteristics

Package (TFBGA)	Power	θ_{JA}	θ_{JB}	θ_{JC}
JH7110	5 W	8.1 ℃/W	1.39 ℃/W	0.46 ℃/W

7.2. Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

7.2.1. Purchasing Information

StarFive JH7110 SoC is purchased by using the product model - JH7110 as the key for ordering.

Table 7-2 Ordering Information

Orderable Device	RoHS	Package	Package Qty	Special Feature
JH7110	RoHS 6/6	FCBGA	900	RISC-V U74 quad-core, GPU IMG BXE-4-32

Note:
The minimum package quantity is 900, however, less than 900 is orderable.

7.2.2. Top Marking

The following figure and table list the top marking information of JH7110.

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Figure 7-1 Top Marking

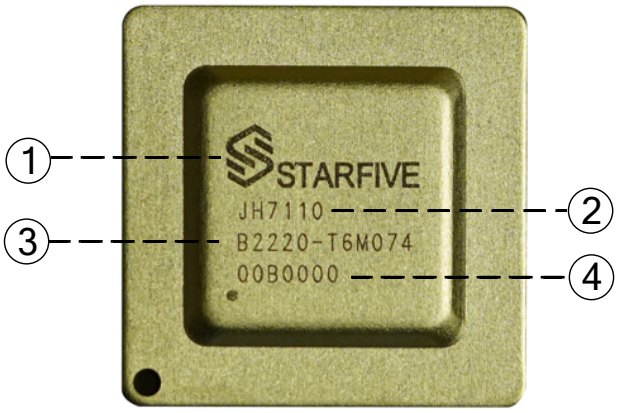

Table 7-3 Marking Definition

Legend	Explanation	Customization
①	StarFive Logo	Customizable
②	Main Product Name - JH7110	Fixed
③	Package ID - BYYWW-XXXXXX • B - Package vendor code • YYWW - Year and Week • XXXXXX - The first 6 digits from wafer lot	NA
④	XXXXXX - The last 7 digits from mes lot	NA

7.2.3. Package Dimensions

The following figures show the package dimension information of JH7110.

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Figure 7-2 Package Top View

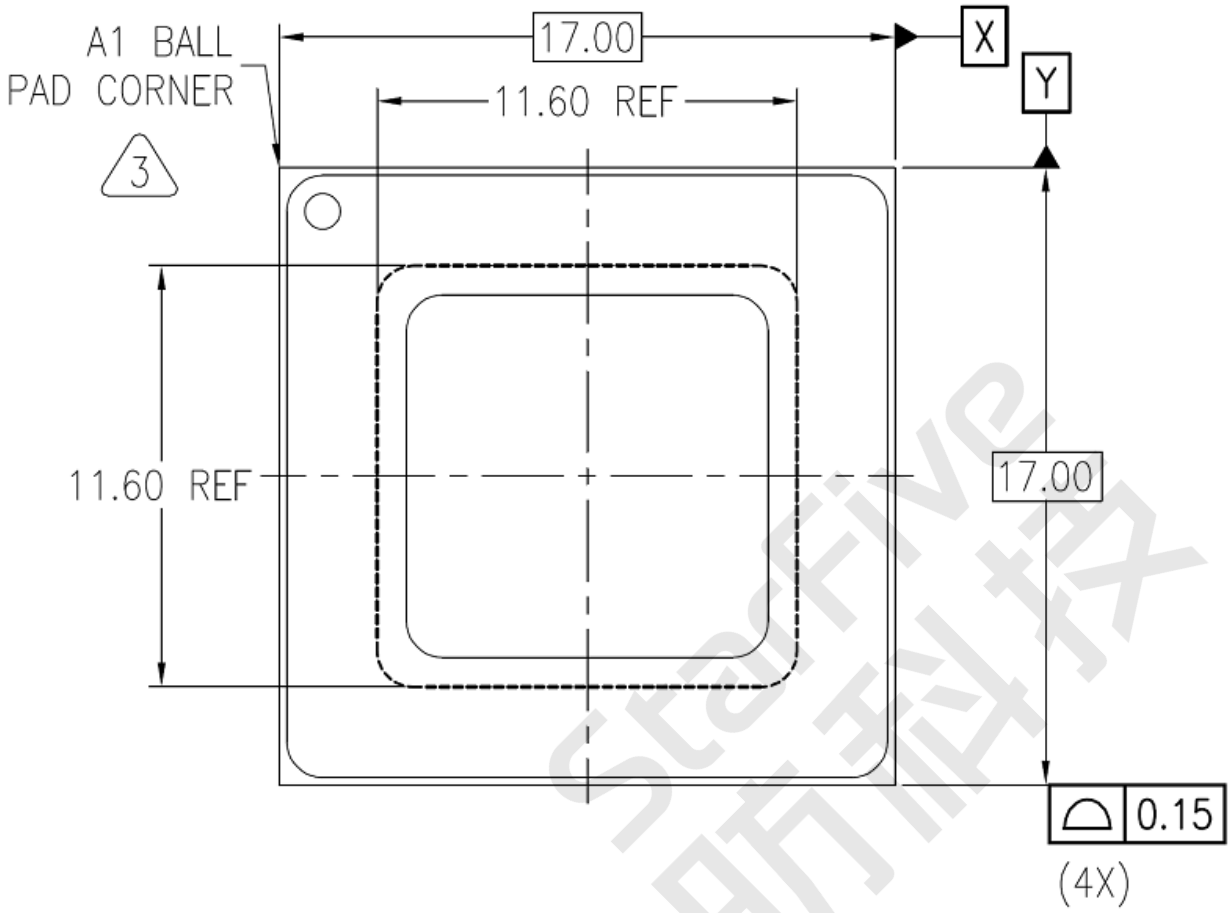

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Figure 7-3 Package Side View

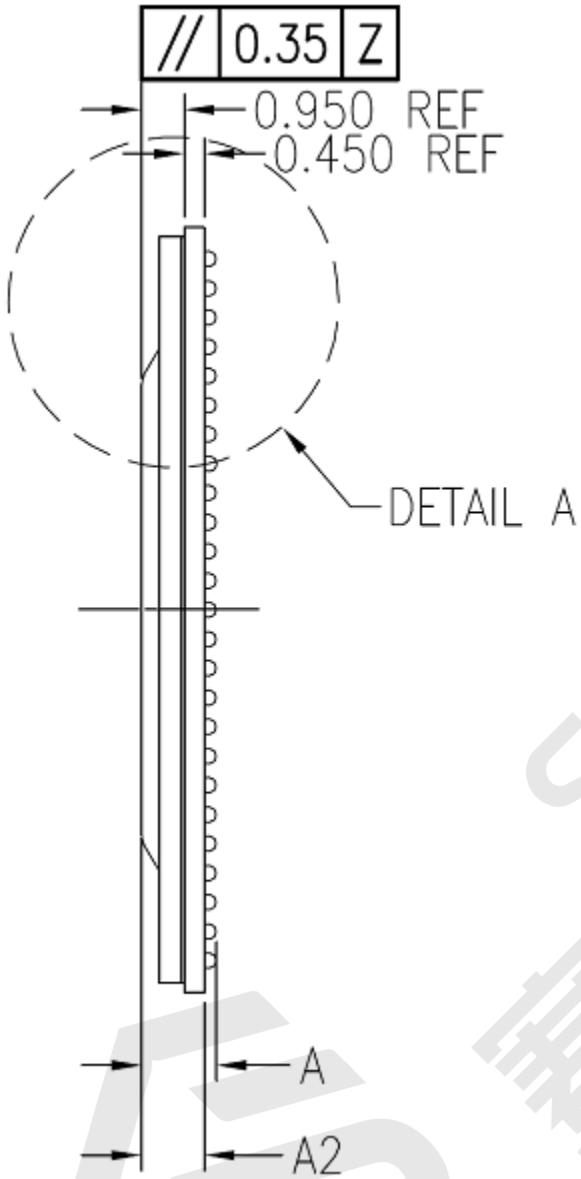

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Figure 7-4 Package Side View Detail A

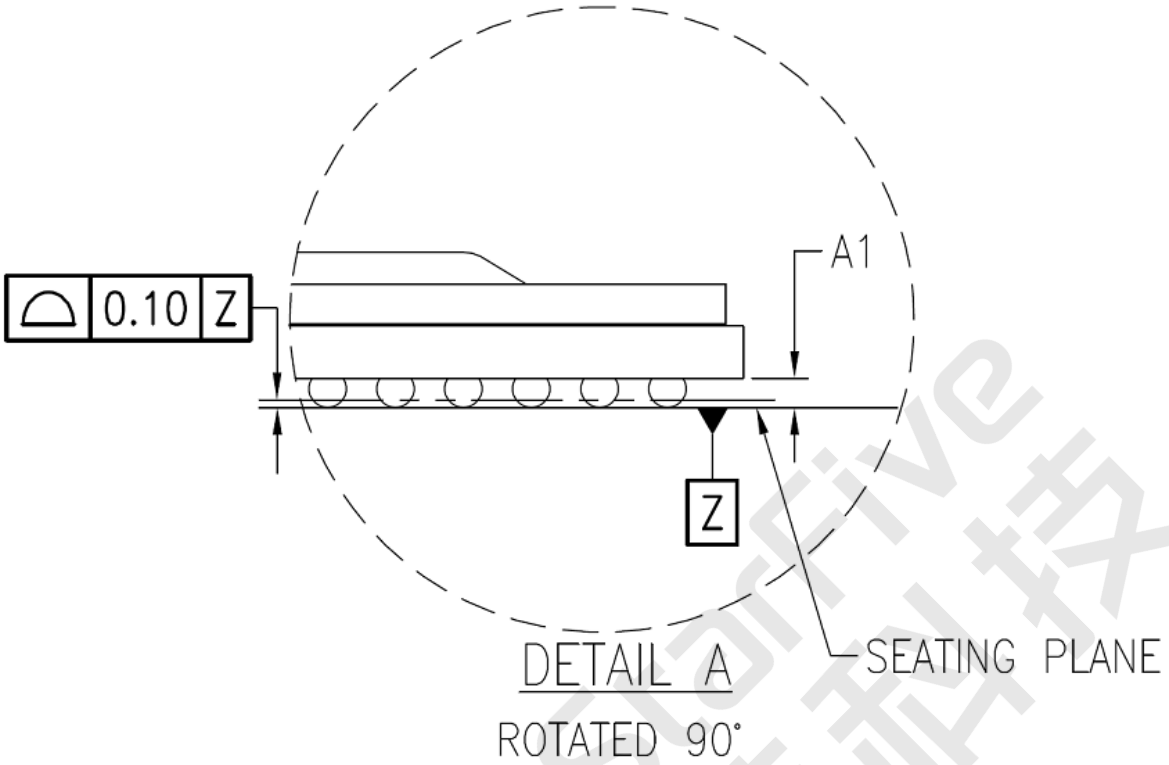

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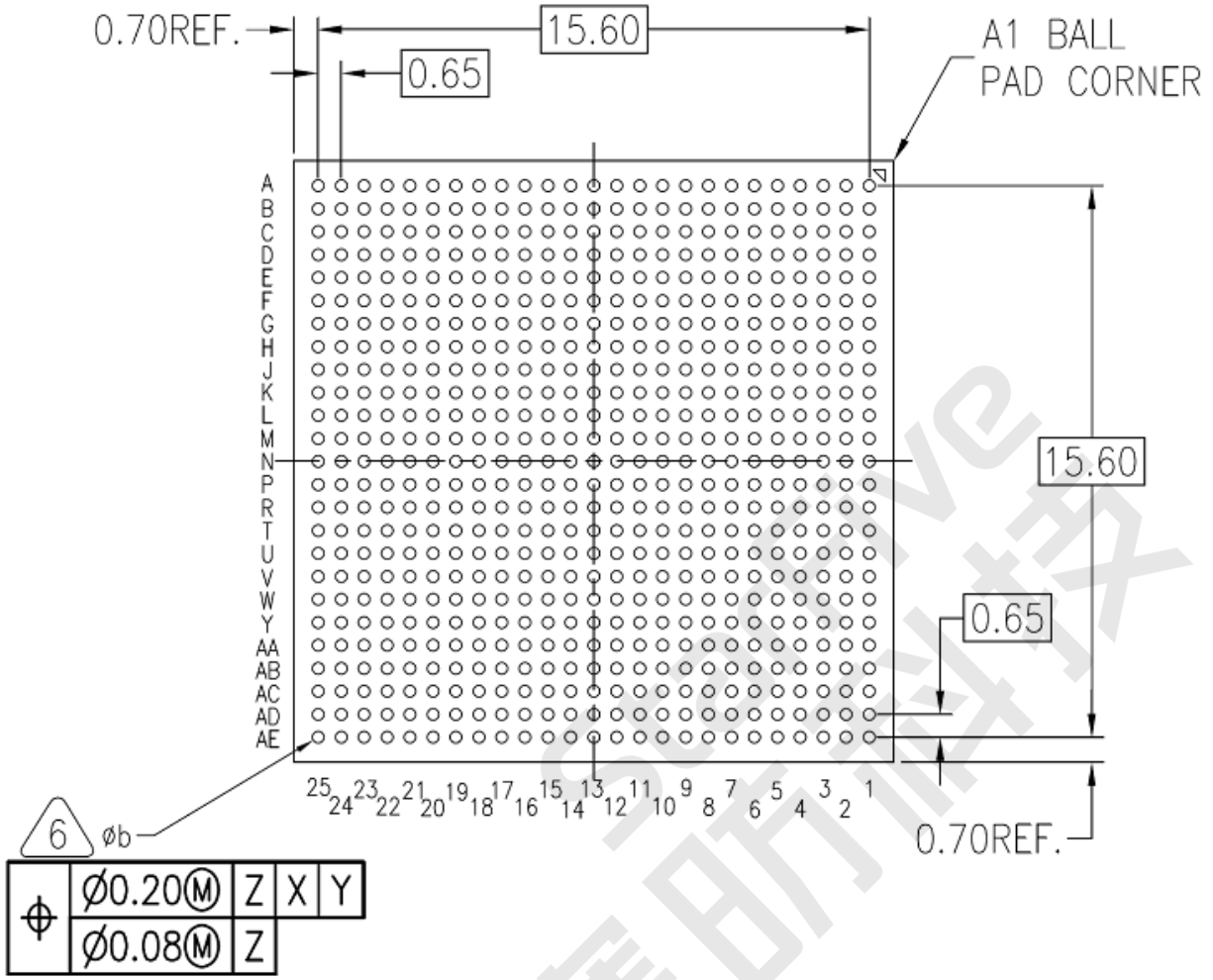
Figure 7-5 Package Bottom View



The following table lists the package dimensions marked in the above diagrams.

Table 7-4 Package Dimensions

Dimension	Minimum	Nominal	Maximum
A	--	1.670	1.761
A1	0.220	0.270	0.320
A2	1.329	1.400	1.476
b	0.300	0.350	0.400
Number of balls: 625			

Note:

1. All dimensions and tolerance conform to the same Y14.5M-2018.
2. Terminal positions designation per JESD 95.
3. Corner as mentioned in Figure 7-2 : Package Top View *(on page 96)* should follow details per StarFive option.
4. Pin 1 identifier can be a chamfer, an ink mark, a lasered mark, or a metallized mark.
5. Ball diameter after reflow.

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6. Dimension "b" as mentioned in Figure 7-5 : Package Bottom View *(on page 99)* is measured at the maximum solder ball diameter parallel to primary Datum C.
7. Use 0.35 mm raw solder ball size during assembly.

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8. Known Issue

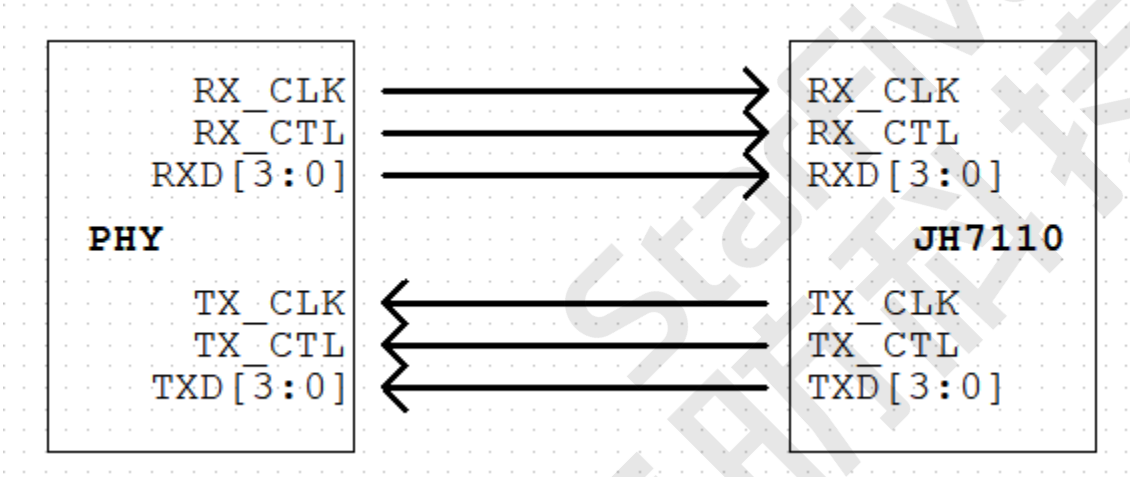
8.1. Ethernet GMAC Supports RGMII Only

JH7110 only supports RGMII mode for Ethernet GMAC connections. Due to this limitation, JH7110 has the following layout requirements.

8.1.1. 1,000 M Only

If you only need to support 1,000 M mode, you can design the layout following the requirements below.

Figure 8-1 GMAC 1,000 M Only



Layout requirements.

- The RX/TX trace length cannot exceed 6,000 mil.
- Match the RXD[3:0] signal group and the RX_CTL and RX_CLK signals with trace length to within 100 mil. Match the TXD[3:0] signal group and the TX_CTL and TX_CLK group trace length to within 100 mil.
- The routing of data and clock lanes should keep a complete reference plane.

8.1.2. Auto-Negotiation

If you need to support 10/100/1,000 M mode auto-negotiation, you need to know the following limitations, and then you can design the layout following the requirements below.

Important:
For auto-negotiation mode, only the following PHY models are supported.

- YT8521DH/DC
- YT8531DH/DC

Plus, you need to connect the RX_CLK of the PHY to its TX_CLK as shown by the orange lines in the following diagram.

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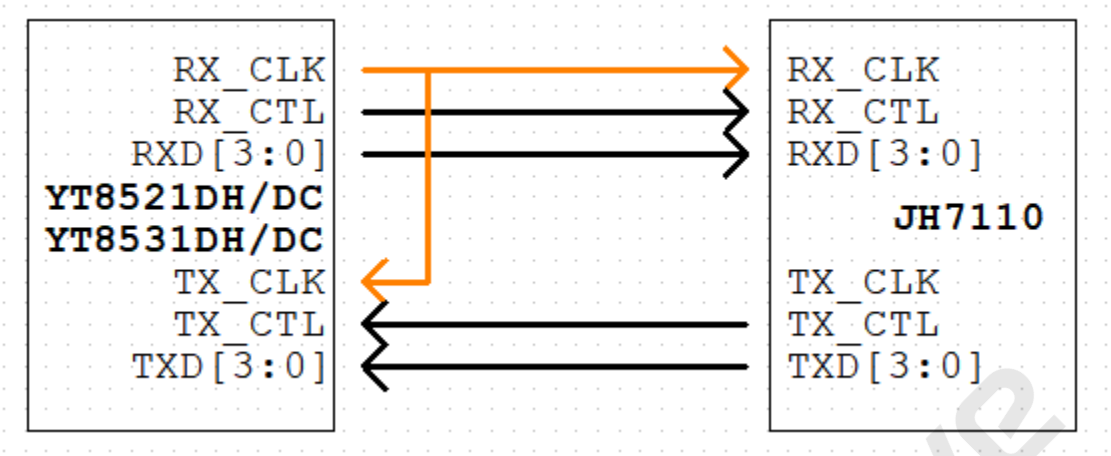
Figure 8-2 GMAC 10 M/100 M/1,000 M Auto-Negotiation



Layout requirements for GMAC0.

- The trace length from TX_CLK to RX_CLK cannot exceed 500 mil.
- The RX and TX trace length cannot exceed 4,300 mil.
- Match the RXD[3:0] signal group and the RX_CTL and RX_CLK signals with trace length to within 100 mil.
- Match the TXD[3:0] signal group and the TX_CTL and RX_CLK signals with trace length to within 100 mil.
- The routing of data and clock lanes should keep a complete reference plane.

Layout requirements for GMAC1.

- The trace length from TX_CLK to RX_CLK cannot exceed 500 mil.
- The RX_CLK trace length cannot exceed 4,000 mil. Match the RXD[3:0] signal group and the RX_CTL and RX_CLK signals with trace length to within 100 mil.
- The TX_CLK trace length is 2,000 mil longer than that of the RX_CLK. Match the TXD[3:0] signal group and the TX_CTL and RX_CLK signals with trace length to within 100 mil.
- The routing of data and clock lanes should keep a complete reference plane.

8.2. Set DDR/LPDDR to 2,133

The DDR and LPDDR of JH7110 is designed to rate up to the speed of 2,800 Mbps, however, the tuning work is not completed yet.

As for now, you are recommended to use maximum rate of 2,133 Mbps, please keep tuned for updates in the Resources *(on page 104)* channels, StarFive will make announcements once the tuning work is completed.

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9. Buy Now

Click on this tab to find all the online shops and compatible accessories.

Buy SBC

Use the following page to find your nearest sales channel or the global channels for purchasing a VisionFive 2 Single Board Computer (SBC).

- Buy VisionFive 2

Buy Parts

Use the following page to find the parts that are tested as compatible with VisionFive 2.

- Buy Accessory

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10. Resources

Click on this tab to find all SBC relevant resources.

StarFive provides the following resources to guide you through an extraordinary experience on using the VisionFive 2 SBC.

- RVspace Wiki
- Application Center
- Documentation Center
- Technical Forum
- VisionFive 2 GitHub Repository
- VisionFive 2 Debian OS Download
- Code download
- View All PDF Documents

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11. Glossary

11.1. AON

Always-On.

11.2. DRAM

Dynamic Random Access Memory.

11.3. eDRAM

Embedded DRAM.

11.4. Instruction Set

A group of commands for a CPU in machine language that can refer to all possible instructions for a CPU, or a subset of instructions to enhance its performance in specific situations, and includes:

- Instruction length - which can vary, Opcodes - the command to be carried out.
- Operands - on which the command will operate.
- Registers - internal locations that are limited in number and ability while quick to access.
- Memory - external storage - a larger and more versatile number of locations that are slower to access.

11.5. ISA

Instruction Set Architecture.

11.6. Latch

A circuit that has two stable states that is used to store state information, known as a bi-stable multi-vibrator.

11.7. LPDDR

Low Power Double Data Rate

11.8. MIPS

Microprocessor without Interlocked Pipelined Stages—a *reduced instruction set computer (RISC)* instruction set architecture developed by MIPS Computer Systems, now MIPS Technologies, based in the United States, that influenced later RISC architectures.

11.9. MMU

Memory Management Unit.

11.10. MODE

A field within an instruction or instruction set that specifies the way the operand or the effective address is determined.

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11.11. MSI

Message Signal Interrupt.

11.12. OS-level Sandboxing

A form of sandboxing implemented by the pointer masking proposal. There is no guarantee that sandboxed code cannot modify the pointer mask and therefore the sandbox does not allow modifying pointer masks in user mode.

11.13. PD

Short for pull down. When talking about PD in circuit layout, it is always used to indicate the need of a pull-down resistor (PD).

Pull-up and Pull-down resistors are used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition

11.14. PLIC

Platform-Level Interrupt Controller. The PLIC is a device designed to handle interrupts other than timer and software in RISC-V.

11.15. Privileged

Provides security isolation, and a means to reduce code defects because code does not have to check for illegal values. Privileged contains state, is used primarily to run applications and can be used to debug implementations. It defines CSR address space and content trap when taken increases privilege mode (say from U to S) trap when taken stays at the current privilege mode access more than even M mode. Its addresses reserved in ISA. address includes highest mode that access the CSR and if it is `r/w/rw/none` preserve bits already there when you change a field.

11.16. Profile

ISA Profile is a set of extensions (instructions, state and behaviors) that users can depend on working together. Extensions are either required, optional, unsupported, or incompatible. RISC-V has defined two Profile types: Application (RVAyy)--appropriate for Linux-class and other embedded designs with more sophisticated ISA needs—and Micro-controller (RVMyy)-- appropriate for cost-sensitive application-optimized embedded designs running bare-metal or simple RTOS environments.

11.17. Pseudo Instructions

In support of a core design goal for RISC-V ISA - high-performance - pseudo instructions often include special commands to the assembler. The use of pseudo instructions supports a policy of keeping the instruction set as small as possible, while supporting optimization and adding clarity to software programming. For example, the use of a pseudo instruction enables loading into memory with a 32-bit offset (called big) that is not directly available, because only 16-bit offsets are permitted.

11.18. PTE

Page Table Entry - an entry in the data structure used by a virtual memory system in a computer operating system to store the mapping between virtual addresses (used by the program executed by the accessing process) and physical addresses (used by the hardware, or more specifically, by the RAM subsystem), that enables access data in memory

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11.19. PU

Short for pull up. When talking about PU in circuit layout, it is always used to indicate the need of a pull-up resistor (PU).

Pull-up and Pull-down resistors are used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition

11.20. PTEP

Parallel Telemetry Processor - a high- speed virtual processor architecture.

11.21. Register

A group of flip-flops with each flip-flop capable of storing one bit of information. The simplest register is one that consists of only flip-flops with no external gates.

11.22. RISC

Reduced Instruction Set Computer architecture. Information processing using any of a family of microprocessors that are designed to execute computing tasks with the simplest instructions in the shortest amount of time possible. RISC-based machines execute one instruction per clock cycle as opposed to CISC (Complex Instruction Set Computer) machines that can have special instructions as well as instructions that take more than one cycle to execute.

11.23. Segmentation fault

A failure condition caused by a memory access violation in hardware operating with memory protection. The fault process notifies the *operating system (OS)* that software has attempted to access a restricted area of memory.

11.24. SHA

Secure Hash Algorithms—a family of cryptographic hash functions published by the National Institute of Standards and Technology as a U.S. Federal Information Processing Standard that started with what is now known as SHA-0, a retronym used for the original (1993) 160-bit hash function published under the name "SHA".

11.25. SoC

System-on-a-Chip.

11.26. SRAM

Static Random Access Memory.

11.27. TRNG

True Random Number Generator - also known as HRNG, or Hardware Random Number Generator - a device that generates random numbers from a physical process, rather than by means of an algorithm. Such devices are often based on microscopic phenomena that generate low-level, statistically random "noise" signals, like thermal noise, the photoelectric effect involving a beam splitter, and other quantum phenomena.

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